



# STIC Search Report

## EIC 2800

STIC Database Tracking Number: 128388

**TO: Monica Lewis**  
**Location:**  
**Art Unit : 2822**  
**Thursday, July 29, 2004**  
**Case Serial Number: 09849537**

**From: Bode Fagbohunka**  
**Location: EIC 2800**  
**Jeff 4A58**  
**Phone: 571-272-2541**  
**bode.fagbohunka@uspto.gov**

### Search Notes

**Examiner Monica Lewis**

Please find attached the results of your search for **09849537**. The search was conducted using the standard collection of databases on dialog for EIC 2800. The tagged references appear to be the closest references located during our search.

If you would like a re-focus please let me know or if you have any questions regarding the search results please do not hesitate to contact me.

Bode Fagbohunka



# STIC Search Results Feedback Form

## EIC 2800

Questions about the scope or the results of the search? Contact *the EIC searcher* or contact:

Jeff Harrison, EIC 2800 Team Leader  
571-272-2511, JEF 4B68

## Voluntary Results Feedback Form

➤ I am an examiner in Workgroup:  Example: 2810

➤ Relevant prior art **found**, search results used as follows:

- ☐ 102 rejection
- ☐ 103 rejection
- ☐ Cited as being of interest.
- ☐ Helped examiner better understand the invention.
- ☐ Helped examiner better understand the state of the art in their technology.

Types of relevant prior art found:

- ☐ Foreign Patent(s)
- ☐ Non-Patent Literature  
(journal articles, conference proceedings, new product announcements etc.)

➤ Relevant prior art **not found**:

- ☐ Results verified the lack of relevant prior art (helped determine patentability).
- ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to STIC/EIC2800, GP4-9C13



Your Name Mihovis Examiner # \_\_\_\_\_

AU 2822 Phone 272-1838 Room 5730

In what format would you like your results? Paper is the default. PAPER DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: \_\_\_\_\_

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. \_\_\_\_\_

What types of references would you like? Please checkmark:

Primary Refs ☒ Nonpatent Literature \_\_\_\_\_ Other \_\_\_\_\_  
Secondary Refs ☒ Foreign Patents \_\_\_\_\_  
Teaching Refs \_\_\_\_\_

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 13, 16, 17 & 52-59

Problem: See pages 2 & 3

Solution: " " 3 & 4

See Figures 9 & 10

Staff Use Only

Searcher: Bode 1-284444 Structure (#) \_\_\_\_\_

Searcher Phone: 22541 Bibliographic ☒

Searcher Location: STIC-EIC2800, JEF-4B68 Litigation \_\_\_\_\_

Type of Search

Vendors

STN \_\_\_\_\_

Dialog ☒

Questel/Orbit \_\_\_\_\_

Set	Items	Description
S1	13907	AU=(ZHANG T? OR ZHANG, T? OR KHAN, R? OR KHAN R?)
S2	22369	BGA? ? OR BALL()GRID?
S3	5756521	SUBSTRAT? OR WAFER? OR IC? ? OR SEMICONDUCTOR? OR SEMI()CO- NDUCTOR?
S4	9379195	FIRST? OR SECOND?
S5	9388376	SURFACE?
S6	8181292	HEAT? OR THERMAL?
S7	568683	SPREAD?
S8	272569	PCB? ? OR PRINT?()CIRCUIT?
S9	23	S1 AND S2
S10	17	S9 AND S7
S11	17	S6 AND S10
S12	15	IDPAT (sorted in duplicate/non-duplicate order)
S13	15	IDPAT (primary/non-duplicate records only)
S14	380824	S4 (10N)S5
S15	12641	S6(6N)S7
S16	8	S14 AND S15 AND S2 AND S3 AND S8
S17	8	RD (unique items)
S18	4	S17 NOT S13
S19	24	S14 AND S15 AND S2 AND (S3 OR S8)
S20	16	S19 NOT S17
S21	16	RD (unique items)
S22	12	S21 NOT S13

? show files

File 2:INSPEC 1969-2004/Jul W3  
(c) 2004 Institution of Electrical Engineers

File 6:NTIS 1964-2004/Jul W4  
(c) 2004 NTIS, Intl Cpyrght All Rights Res

File 8:Ei Compendex(R) 1970-2004/Jul W3  
(c) 2004 Elsevier Eng. Info. Inc.

File 34:SciSearch(R) Cited Ref Sci 1990-2004/Jul W3  
(c) 2004 Inst for Sci Info

File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec  
(c) 1998 Inst for Sci Info

File 99:Wilson Appl. Sci & Tech Abs 1983-2004/Jun  
(c) 2004 The HW Wilson Co.

File 94:JICST-EPlus 1985-2004/Jul W1  
(c) 2004 Japan Science and Tech Corp(JST)

File 92:IHS Intl.Stds.& Specs. 1999/Nov  
(c) 1999 Information Handling Services

File 144:Pascal 1973-2004/Jul W3  
(c) 2004 INIST/CNRS

File 647:CMP Computer Fulltext 1988-2004/Jul W3  
(c) 2004 CMP Media, LLC

File 696:DIALOG Telecom. Newsletters 1995-2004/Jul 23  
(c) 2004 The Dialog Corp.

File 35:Dissertation Abs Online 1861-2004/May  
(c) 2004 ProQuest Info&Learning

File 65:Inside Conferences 1993-2004/Jul W4  
(c) 2004 BLDSC all rts. reserv.

File 103:Energy SciTec 1974-2004/Jul B1  
(c) 2004 Contains copyrighted material

File 350:Derwent WPIX 1963-2004/UD,UM &UP=200447  
(c) 2004 Thomson Derwent

File 347:JAPIO Nov 1976-2004/Mar(Updated 040708)  
(c) 2004 JPO & JAPIO

File 202:Info. Sci. & Tech. Abs. 1966-2004/Jul 12  
(c) 2004 EBSCO Publishing

File 239:Mathsci 1940-2004/Sep

(c) 2004 American Mathematical Society  
File 95:TEME-Technology & Management 1989-2004/Jun W1  
(c) 2004 FIZ TECHNIK  
File 25:Weldasearch 1966-2003/Dec  
(c) 2004 TWI Ltd  
File 62:SPIN(R) 1975-2004/May W5  
(c) 2004 American Institute of Physics  
File 96:FLUIDEX 1972-2004/Jul  
(c) 2004 Elsevier Science Ltd.  
File 98:General Sci Abs/Full-Text 1984-2004/Jun  
(c) 2004 The HW Wilson Co.  
File 266:FEDRIP 2004/Jun  
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13/9/1 (Item 1 from file: 350)  
DIALOG(R) File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

016340107 \*\*Image available\*\*  
WPI Acc No: 2004-498004/200447  
Related WPI Acc No: 2004-009777  
XRAM Acc No: C04-184418  
XRPX Acc No: N04-393271

**Integrated circuit package, e.g. ball grid array package for die-up and die-down orientations, comprises first substrate surface attached to first surface of stiffener, and second substrate surface attached to second surface of stiffener**

Patent Assignee: BROADCOM CORP (BROA-N)  
Inventor: CHAUDHRY I; KHAN R R ; ZHAO S Z  
Number of Countries: 001 Number of Patents: 001  
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20040113284	A1	20040617	US 2002101751	A	20020321	200447 B
			US 2003730093	A	20031209	

Priority Applications (No Type Date): US 2002101751 A 20020321; US 2003730093 A 20031209

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040113284	A1	52	H01L-023/48	Div ex application	US 2002101751

Abstract (Basic): US 20040113284 A1

NOVELTY - An integrated circuit (IC) package comprises first substrate (104); second substrate (502); and stiffener (112).

A surface of the first substrate is attached to a first surface of the stiffener, and a surface of the second substrate is attached to a second surface of the stiffener.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(a) a method of assembling a **ball grid array ( BGA )** package (402, 500) comprising attaching a surface of a first substrate to a first surface of a stiffener; and attaching a surface of a second substrate to a second surface of the stiffener; and

(b) a method of making IC packages comprising forming a stiffener strip that includes stiffeners; forming a first substrate strip that includes first substrates; forming a second substrate strip that includes second substrates; laminating the first substrate strip to a first surface of the stiffener strip; and laminating the second substrate strip to a second surface of the stiffener strip, where a substrate/stiffener/substrate strip combination is created.

USE - The IC package, e.g. **BGA** package is used for die-up and die-down orientations.

ADVANTAGE - The IC package has improved **heat - spreading** capabilities while providing greater routing capacity and higher levels of IC electrical performance.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a **BGA** package.

Package (100)

Die (102)

Substrate (104, 502)

Stiffener (112)

**Thermal** connector (404)

**BGA** package (500)

pp; 52 DwgNo 5/21

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: A second surface of the second substrate has a central region that allows the attachment. The second substrate has a centrally located opening configured to allow an IC die (102) to attach to the second surface of the stiffener through the centrally located opening. The package further comprises a conductive material in the via. It further comprises a **thermal** connector (404) that has a first surface coupled to the first surface of the stiffener through the centrally located opening. It further comprises a solder ball attached to each of the solder ball pads. It further comprises an IC die attached to the second surface of the second substrate in the central region; and an electronic device attached to the second surface of the second substrate. A second surface of the **thermal** connector is configured to be coupled to a printed circuit board. A solder or silver-filled epoxy is used to couple the first surface of the **thermal** connector to the first surface of the stiffener.

Title Terms: INTEGRATE; CIRCUIT; PACKAGE; BALL; GRID; ARRAY; PACKAGE; DIE; UP; DIE; DOWN; ORIENT; COMPRISE; FIRST; SUBSTRATE; SURFACE; ATTACH; FIRST; SURFACE; STIFFEN; SECOND; SUBSTRATE; SURFACE; ATTACH; SECOND; SURFACE; STIFFEN

Derwent Class: A21; A85; L03; U11; V04

International Patent Class (Main): H01L-023/48

International Patent Class (Additional): H01L-021/44; H01L-029/40

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A12-E07C; L04-C17A; L04-F02; L04-F03

Manual Codes (EPI/S-X): U11-D01A3; U11-D01A5; U11-D02B1; U11-E02A2;

V04-T03A

Polymer Indexing (PS):

<01>

\*001\* 2004; P0464-R D01 D22 D42 F47; K9449

\*002\* 2004; ND01; K9449; K9416; Q9999 Q7476 Q7330

\*003\* 2004; Ag 1B Tr; R05319 D00 D09 Ag; A999 A237

13/9/2 (Item 2 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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016098206 \*\*Image available\*\*

WPI Acc No: 2004-256082/200424

Related WPI Acc No: 2002-635363; 2002-635365; 2003-420004; 2003-620193;

2003-678809; 2003-678811; 2003-678812; 2003-720751; 2004-080035;

2004-080038; 2004-080065; 2004-080066; 2004-256081

XRAM Acc No: C04-099952

XRPX Acc No: N04-203516

Ball grid array package for printed circuit board, has solder balls attached to bottom of tape substrate mounted with stiffener, integrated circuit die and heat spreader, sequentially

Patent Assignee: KHAN R R (KHAN-I); ZHAO S Z (ZHAO-I)

Inventor: KHAN R R ; ZHAO S Z

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020185722	A1	20021212	US 2000742366	A	20001222	200424 B
			US 2002201891	A	20020725	

Priority Applications (No Type Date): US 2000742366 A 20001222; US

2002201891 A 20020725

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

US 20020185722 A1 37 H01L-023/02 Div ex application US 2000742366

Abstract (Basic): US 20020185722 A1

NOVELTY - A tape substrate (104) is mounted with the stiffener, integrated circuit (IC) die (102) and **heat spreader**, sequentially. Several solder balls (106) are attached to the bottom of the substrate.

DETAILED DESCRIPTION - The **heat spreader** dissipates **heat** generated by IC die attached through silver filled epoxy (116). The **heat spreader** contact area of die, is greater than that of **heat spreader**. The **heat spreader** has a surface which forms specific exposed surface of the package. An INDEPENDENT CLAIM is also included for assembling method of **ball grid array (BGA)** package which involves reducing **thermal** stress at interface of IC die and stiffener surface, during operation of die.

USE - For printer circuit board.

ADVANTAGE - Improves IC electrical performance and **heat spreading** capabilities of the package.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the **BGA** package.

IC die (102)  
substrate (104)  
solder balls (106)  
**BGA** package (110)  
stiffener (112)  
openings (114)  
silver filled epoxy (116)  
pp; 37 DwgNo 1B/21

Title Terms: BALL; GRID; ARRAY; PACKAGE; PRINT; CIRCUIT; BOARD; SOLDER; BALL; ATTACH; BOTTOM; TAPE; SUBSTRATE; MOUNT; STIFFEN; INTEGRATE; CIRCUIT; DIE; **HEAT**; **SPREAD**; SEQUENCE

Derwent Class: A85; L03; U11; V04

International Patent Class (Main): H01L-023/02

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A12-E07A; L04-C21; L04-C25

Manual Codes (EPI/S-X): U11-D01A3; U11-D02B1; U11-E02A1; V04-T03A

Polymer Indexing (PS):

<01>

\*001\* 2004; P0464-R D01 D22 D42 F47; K9449

\*002\* 2004; Q9999 Q7454 Q7330; Q9999 Q7476 Q7330; Q9999 Q6644-R; Q9999 Q7669; ND01; K9449

\*003\* 2004; R05319 D00 D09 Ag; A999 A237

13/9/3 (Item 3 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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016098205 \*\*Image available\*\*

WPI Acc No: 2004-256081/200424

Related WPI Acc No: 2002-635363; 2002-635365; 2003-420004; 2003-620193;

2003-678809; 2003-678811; 2003-678812; 2003-720751; 2004-080035;

2004-080038; 2004-080065; 2004-080066; 2004-256082

XRAM Acc No: C04-099951

XRPX Acc No: N04-203515

**Ball - grid array package for high-speed application specific integrated circuit, has heat spreader mounted on integrated circuit die, dissipates heat generated by die**

Patent Assignee: BACHER B (BACH-I); KHAN R R (KHAN-I); ZHAO S Z (ZHAO-I)

Inventor: BACHER B; KHAN R R; ZHAO S Z

Number of Countries: 001 Number of Patents: 001

Patent Family:



Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020185720	A1	20021212	US 2000742366	A	20001222	200424 B
			US 2002197438	A	20020718	

Priority Applications (No Type Date): US 2000742366 A 20001222; US 2002197438 A 20020718

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 20020185720	A1	36	H01L-023/02	Div ex application US 2000742366

Abstract (Basic): US 20020185720 A1

NOVELTY - A tape/organic substrate (104) has stiffener (112) on which an integrated circuit (IC) die (102) is mounted by silver filled epoxy (116). A **heat spreader** (402) mounted on die center dissipates **heat** generated by die. Several solder balls (106) connected to ground potential, are attached to substrate lower surface and to stiffener through a conductive material filled via extending through substrate.

DETAILED DESCRIPTION - The wire bonds (108) provided corresponding to bond pads (118) formed on IC die, couples bond pad to stiffener lower surface into which an opening (114) is extending from upper surface. Another wire bond couples another bond pad to metal layer by extending through the stiffener openings so as to connect to substrate via. The substrate has window opening which exposes portion of stiffener lower surface which is configured to be coupled with printed circuit board (PCB) such that the PCB is coupled to **heat spreader** whose upper surface is plated with solder. The stiffener has a centrally-located cavity which protrudes through window opening and which is plated with solder such that the stiffener is surface mounted to soldering pad of PCB. A metal ring is attached to stiffener upper surface to which ground pad of IC die is coupled by ground wire bond, so as to dissipate **heat** from stiffener. A stud bridges stiffener across wire bond opening extending through stiffener. A plated die-attach pad centered on the substrate, is configured to mount the IC die. An INDEPENDENT CLAIM is also included for **ball grid array** package assembling method.

USE - **Ball grid array ( BGA )** package e.g. ceramic **BGA** package, plastic **BGA** (PBGA) package, flex **BGA** package, die-up and die-down **BGA** packages, for high speed application specific integrated circuits (ASIC).

ADVANTAGE - By providing the **heat spreader**, the **heat spreading** and dissipating capabilities are improved.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of die-up flex **BGA** package.

- IC die (102)
- tape/organic substrate (104)
- solder balls (106)
- wire bonds (108)
- stiffener (112)
- epoxy (116,404)
- stiffener openings (114)
- bond pads (118)
- contact points (120)
- heat spreader** (402)

pp; 36 DwgNo 4/21

Title Terms: BALL; GRID; ARRAY; PACKAGE; HIGH; SPEED; APPLY; SPECIFIC; INTEGRATE; CIRCUIT; **HEAT**; **SPREAD**; MOUNT; INTEGRATE; CIRCUIT; DIE; DISSIPATE; **HEAT**; GENERATE; DIE

Derwent Class: A85; L03; U11; V04

International Patent Class (Main): H01L-023/02

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A05-A01E2; A12-E07C; L04-C21; L04-C25  
Manual Codes (EPI/S-X): U11-D01A3; U11-D02B1; U11-D03A2; U11-E02A1;  
V04-T03A  
Polymer Indexing (PS):

<01>

\*001\* 2004; P0464-R D01 D22 D42 F47; K9449  
\*002\* 2004; ND01; K9449; Q9999 Q7476 Q7330; B9999 B5527 B5505  
\*003\* 2004; R05319 D00 D09 Ag; A999 A237

13/9/4 (Item 4 from file: 350)  
DIALOG(R) File 350:Derwent WPIX  
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015922226 \*\*Image available\*\*  
WPI Acc No: 2004-080066/200408  
Related WPI Acc No: 2002-635363; 2002-635365; 2003-420004; 2003-620193;  
2003-678809; 2003-678811; 2003-678812; 2003-720751; 2004-080035;  
2004-080038; 2004-080065; 2004-256081; 2004-256082  
XRAM Acc No: C04-032728  
XRPX Acc No: N04-063959

Die-up flex ball grid array package has heat spreader mounted on  
integrated circuit die that is mounted on stiffener  
Patent Assignee: BACHER B (BACH-I); KHAN R R (KHAN-I); ZHAO S Z (ZHAO-I)  
Inventor: BACHER B; KHAN R R ; ZHAO S Z  
Number of Countries: 001 Number of Patents: 001  
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020190362	A1	20021219	US 2000742366	A	20001222	200408 B
			US 2002201309	A	20020724	

Priority Applications (No Type Date): US 2000742366 A 20001222; US  
2002201309 A 20020724

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020190362	A1		37	H01L-023/02	Div ex application US 2000742366

Abstract (Basic): US 20020190362 A1

NOVELTY - A heat spreader (402) is mounted on an integrated circuit (IC) die (102) that is mounted on a stiffener (112).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for ball grid array package assembling method.

USE - Ball grid array package with heat spreader .

ADVANTAGE - The thermal stress and heat at the IC die or stiffener interface is released or altered with introduction of the heat spreader on the top surface of the IC die so packages with improved electrical and thermal characteristics are obtained and also packaging of large sized dies with high input and output counts using ball grid array ( BGA ) technology is enabled.

DESCRIPTION OF DRAWING(S) - The figure illustrates a cross-section of the die-up flex BGA package.

Integrated circuit die (102)

Stiffener (112)

Heat spreader (402)

pp; 37 DwgNo 4/21

Title Terms: DIE; UP; FLEX; BALL; GRID; ARRAY; PACKAGE; HEAT ; SPREAD ;  
MOUNT; INTEGRATE; CIRCUIT; DIE; MOUNT; STIFFEN

Derwent Class: A85; L03; U11; V04

International Patent Class (Main): H01L-023/02

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A12-E07C; L04-C25; L04-F02  
Manual Codes (EPI/S-X): U11-D01A3; U11-D01A5; U11-D01C6; U11-D02B1;  
U11-E02A1; V04-Q02A  
Polymer Indexing (PS):

<01>

\*001\* 2004; P0464-R D01 D22 D42 F47

\*002\* 2004; ND01; Q9999 Q6644-R; Q9999 Q7476 Q7330; K9483-R; K9449

\*003\* 2004; Ag 1B Tr; A999 A237

13/9/5 (Item 5 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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015922225 \*\*Image available\*\*

WPI Acc No: 2004-080065/200408

Related WPI Acc No: 2002-635363; 2002-635365; 2003-420004; 2003-620193;

2003-678809; 2003-678811; 2003-678812; 2003-720751; 2004-080035;

2004-080038; 2004-080066; 2004-256081; 2004-256082

XRAM Acc No: C04-032727

XRPX Acc No: N04-063958

**Die-up ball grid array package for integrated circuit includes heat spreader and solder balls mounted and attached on upper and lower surfaces of integrated circuit die and tape substrate**

Patent Assignee: KHAN R R (KHAN-I); ZHAO S Z (ZHAO-I)

Inventor: KHAN R R ; ZHAO S Z

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020190361	A1	20021219	US 2000742366	A	20001222	200408 B
			US 2002200255	A	20020723	

Priority Applications (No Type Date): US 2000742366 A 20001222; US

2002200255 A 20020723

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020190361	A1		37	H01L-023/02	Div ex application US 2000742366

Abstract (Basic): US 20020190361 A1

NOVELTY - An integrated circuit die (102) is arranged on an upper surface of a stiffener (112) which is mounted on the upper surface of a tape substrate (104). A **heat spreader** (402) is mounted on the surface of the integrated circuit (IC) die. The solder balls (106) are attached to the lower surface of the substrate

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for **ball grid array package assembly**.

USE - Used in field of integrated circuit (IC) device packaging technology e.g. for IC dies using printed circuit board.

ADVANTAGE - **Thermal** stress at the interface of the IC die and stiffener can be substantially released or altered by **heat spreader** and the deformation caused by **thermal** stress in the stiffener and substrate can also be reduced.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of the die up flexible **ball grid array package**.

Integrated circuit die (102)

Tape substrate (104)

Solder ball (106)

Stiffener (112)

**Heat spreader** (402)

pp; 37 DwgNo 4/21

Title Terms: DIE; UP; BALL; GRID; ARRAY; PACKAGE; INTEGRATE; CIRCUIT; **HEAT**  
; **SPREAD** ; SOLDER; BALL; MOUNT; ATTACH; UPPER; LOWER; SURFACE; INTEGRATE  
; CIRCUIT; DIE; TAPE; SUBSTRATE

Derwent Class: A85; L03; U11; V04

International Patent Class (Main): H01L-023/02

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A12-E07C; L04-C17A; L04-F02

Manual Codes (EPI/S-X): U11-D01A3; U11-D01A5; U11-D01C6; U11-D02B1;

U11-D03B3; V04-Q02A

Polymer Indexing (PS):

<01>

\*001\* 2004; P0464-R D01 D22 D42 F47

\*002\* 2004; ND01; Q9999 Q6644-R; Q9999 Q7476 Q7330; K9483-R; K9449

\*003\* 2004; Ag 1B Tr; A999 A237

13/9/6 (Item 6 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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015922198 \*\*Image available\*\*

WPI Acc No: 2004-080038/200408

Related WPI Acc No: 2002-635363; 2002-635365; 2003-420004; 2003-620193;

2003-678809; 2003-678811; 2003-678812; 2003-720751; 2004-080035;

2004-080065; 2004-080066; 2004-256081; 2004-256082

XRAM Acc No: C04-032700

XRPX Acc No: N04-063940

Ball grid array package for integrated circuit devices, has  
substrate, stiffener, integrated circuit die, heat spreader, and  
solder balls

Patent Assignee: BACHER B (BACH-I); KHAN R R (KHAN-I); ZHAO S Z (ZHAO-I)

Inventor: BACHER B; KHAN R R ; ZHAO S Z

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020185750	A1	20021212	US 2000742366	A	20001222	200408 B
			US 2002200336	A	20020723	

Priority Applications (No Type Date): US 2000742366 A 20001222; US  
2002200336 A 20020723

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 20020185750	A1	37	H01L-023/48	Div ex application US 2000742366

Abstract (Basic): US 20020185750 A1

NOVELTY - An electrically and **thermally** enhanced die-up tape  
substrate **ball grid array ( BGA )** package and die-up plastic  
substrate **BGA** package.

DETAILED DESCRIPTION - A **BGA** package comprises:

- (i) a substrate that has a first and second surface;
- (ii) a stiffener that has a first and second surface joined to  
substrate;
- (iii) an IC die mounted on first stiffener surface;
- (iv) a **heat** sink mounted on second IC surface;
- (v) a number of solder balls joined to second substrate surface.

The package comprises silver-filled epoxy.

USE - An electrically and **thermally** enhanced die-up tape  
substrate **ball grid array ( BGA )** package and die-up plastic  
substrate **BGA** package.

ADVANTAGE - Assembly has reduced **thermal** stress between

components with different **thermal** co-efficients due to **heat** dissipation.

DESCRIPTION OF DRAWING(S) - Drawing shows conventional flex **BGA** package.

- (100) Flex **BGA** package;
- (102) IC die;
- (104) tape substrate;
- (106) solder balls;
- (108) wire bonds;
- (116) epoxy;
- (118) bond pads;
- (120) contact points.

pp; 37 DwgNo 1/21

Title Terms: BALL; GRID; ARRAY; PACKAGE; INTEGRATE; CIRCUIT; DEVICE;  
SUBSTRATE; STIFFEN; INTEGRATE; CIRCUIT; DIE; **HEAT** ; **SPREAD** ; SOLDER;  
BALL

Derwent Class: A85; L03; U11

International Patent Class (Main): H01L-023/48

International Patent Class (Additional): H01L-023/52; H01L-029/40

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A05-A01E2; A08-R05; A12-E07; L03-H04E; L04-C17;  
L04-C25

Manual Codes (EPI/S-X): U11-D01A3; U11-D01A5; U11-D02B; U11-E02A9

Polymer Indexing (PS):

<01>

\*001\* 2004; P0464-R D01 D22 D42 F47

\*002\* 2004; K9449; Q9999 Q7454 Q7330; ND01

\*003\* 2004; R05319 D00 D09 Ag; A999 A237

13/9/7 (Item 7 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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015922195 \*\*Image available\*\*

WPI Acc No: 2004-080035/200408

Related WPI Acc No: 2002-635363; 2002-635365; 2003-420004; 2003-620193;

2003-678809; 2003-678811; 2003-678812; 2003-720751; 2004-080038;

2004-080065; 2004-080066; 2004-256081; 2004-256082

XRAM Acc No: C04-032697

XRPX Acc No: N04-063937

Ball grid array package for integrated circuit devices, has  
substrate, stiffener, integrated circuit die, heat spreader , and  
solder balls

Patent Assignee: KHAN R R (KHAN-I); ZHAO S Z (ZHAO-I)

Inventor: **KHAN R R** ; ZHAO S Z

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020185734	A1	20021212	US 2000742366	A	20001222	200408 B
			US 2002201893	A	20020725	

Priority Applications (No Type Date): US 2000742366 A 20001222; US

2002201893 A 20020725

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 20020185734	A1	37	H01L-021/48	Div ex application US 2000742366

Abstract (Basic): US 20020185734 A1

NOVELTY - **BGA** package comprises: a substrate (104) with first and

second surfaces; a stiffener (112); an IC die (102) with a first surface mounted to the stiffener surface; a **heat spreader** mounted to the die; and solder balls (106) attached to the second substrate surface.

DETAILED DESCRIPTION - AN INDEPENDENT CLAIM is also included for: a method of assembling a **ball grid** array package, which comprises: providing a tape substrate (104) with the two surfaces; attaching the first surface of the stiffener (112) to the first substrate surface; mounting an IC die (102) to the second stiffener surface; mounting a **heat spreader** to the IC die; and attaching a number of solder balls to the second substrate surface.

USE - For substrate stiffening and **heat spreading** techniques in BGA packages.

ADVANTAGE - High levels of IC electrical performance are attained.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a BGA package, with the **heat spreader** internal to the package.

IC die (102)  
substrate (104)  
solder balls (106)  
stiffener (112)  
bond pads on IC die (118)  
contact points on substrate (120)  
pp; 37 DwgNo 5/21

Title Terms: BALL; GRID; ARRAY; PACKAGE; INTEGRATE; CIRCUIT; DEVICE;  
SUBSTRATE; STIFFEN; INTEGRATE; CIRCUIT; DIE; **HEAT** ; **SPREAD** ; SOLDER;  
BALL

Derwent Class: A85; L03; U11

International Patent Class (Main): H01L-021/48

International Patent Class (Additional): H01L-023/48; H01L-029/40

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A12-E07; L04-C17A; L04-C21

Manual Codes (EPI/S-X): U11-D02B; U11-E02A9

Polymer Indexing (PS):

<01>

\*001\* 2004; P0000

\*002\* 2004; Q9999 Q7454 Q7330; Q9999 Q7330-R; ND01

13/9/8 (Item 8 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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015851950 \*\*Image available\*\*

WPI Acc No: 2004-009777/200401

Related WPI Acc No: 2004-498004

XRAM Acc No: C04-002632

XRPX Acc No: N04-007007

Ball grid array package for high-speed integrated circuits, has first substrate surface attached to first stiffener surface, and second substrate surface attached to second stiffener surface

Patent Assignee: BROADCOM CORP (BROA-N)

Inventor: CHAUDHRY I; KHAN R R ; ZHAO S Z

Number of Countries: 032 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030179556	A1	20030925	US 2002101751	A	20020321	200401 B
EP 1351293	A2	20031008	EP 20036501	A	20030321	200401

Priority Applications (No Type Date): US 2002101751 A 20020321

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes  
US 20030179556 A1 52 H05K-007/06  
EP 1351293 A2 E H01L-023/31  
Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB  
GR HU IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR

Abstract (Basic): US 20030179556 A1

NOVELTY - A **ball grid array ( BGA )** package comprises two substrates (104, 502), and a stiffener (112). A surface of the first substrate is attached to a first surface of the stiffener, and a surface of the second substrate is attached to a second surface of the stiffener.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for assembling a **BGA** package.

USE - Used for high-speed ICs.

ADVANTAGE - The **BGA** packages have improved **heat spreading** capabilities, greater routing capacity and higher levels of IC electrical performance.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a **BGA** package.

IC die (102)

Solder ball (106, 304)

Wire bond (108, 306, 806)

Via (302, 816)

pp; 52 DwgNo 8/21

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: A second surface of the second substrate has a central region that allows the attachment of an integrated circuit (IC) die (102). The second substrate has a centrally located opening to allow an IC die to attach to the second surface of the stiffener through the centrally located opening. The second surface of the stiffener is plated with a centrally located metal die-attach pad for attachment of the IC die. The first substrate includes via(s) (302, 816) through the first substrate. The first substrate has a second surface including solder ball (106, 304) pads. A conductive material in via(s) is provided. The package further comprises a **thermal** connector that has a first surface coupled to the first surface of the stiffener through the centrally located opening, where a second surface of the **thermal** connector is coupled to a printed circuit board. The second substrate has opening(s) that exposes a portion of the second surface of the stiffener. The second substrate has an edge formed to expose a portion of the second surface of the stiffener. Wire bond(s) (108, 306, 806) that couples the IC die to a second surface of the second substrate is provided. A resistor, a capacitor, an inductor, or a second IC die is mounted to a second surface of the second substrate.

POLYMERS - Preferred Component: A solder or silver-filled epoxy is used to couple the first surface of the **thermal** connector to the first surface of the stiffener.

Title Terms: BALL; GRID; ARRAY; PACKAGE; HIGH; SPEED; INTEGRATE; CIRCUIT; FIRST; SUBSTRATE; SURFACE; ATTACH; FIRST; STIFFEN; SURFACE; SECOND; SUBSTRATE; SURFACE; ATTACH; SECOND; STIFFEN; SURFACE

Derwent Class: A85; L03; U11; U13; V04

International Patent Class (Main): H01L-023/31; H05K-007/06

International Patent Class (Additional): H01L-023/495

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A12-E07C; L04-F05

Manual Codes (EPI/S-X): U11-D01A3; U11-D02B1; U11-E02A3; U13-E01; V04-T01

Polymer Indexing (PS):

<01>

\*001\* 018; P0464-R D01 D22 D42 F47

\*002\* 018; ND01; Q9999 Q7476 Q7330; Q9999 Q7465 Q7330; Q9999 Q7363 Q7330;  
Q9999 Q6644-R; N9999 N5721-R; K9449; K9483-R  
\*003\* 018; R05319 D00 D09 Ag; A999 A237

13/9/9 (Item 9 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
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015616652 \*\*Image available\*\*  
WPI Acc No: 2003-678809/200364  
Related WPI Acc No: 2002-635363; 2002-635365; 2003-420004; 2003-620193;  
2003-678811; 2003-678812; 2003-720751; 2004-080035; 2004-080038;  
2004-080065; 2004-080066; 2004-256081; 2004-256082  
XRPX Acc No: N03-541939

Stiffener in ball grid array package, has openings with recessed step region provided to its planar top surface

Patent Assignee: BROADCOM CORP (BROA-N)

Inventor: KHAN R R ; ZHAO S Z

Number of Countries: 032 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030146503	A1	20030807	US 2002352877	P	20020201	200364 B
			US 2002284371	A	20021031	
EP 1361611	A2	20031112	EP 20031958	A	20030130	200377

Priority Applications (No Type Date): US 2002352877 P 20020201; US 2002284371 A 20021031

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030146503	A1		25	H01L-023/10	Provisional application US 2002352877

EP 1361611 A2 E H01L-023/498

Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR

Abstract (Basic): US 20030146503 A1

NOVELTY - Several openings (114a,114c) having recessed step regions (606a,606c) at edge portions, are provided to the planar top surface (602) of the stiffener (600).

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) ball grid array package; and

(2) assembling method of ball grid array package.

USE - Stiffener in ball grid array package (claimed).

ADVANTAGE - The recesses step region in the opening of the stiffener, reduces wire bond contact risk during integrated circuit die encapsulation process such as stamping, etching, machining and molding. Improves heat spreading mechanical and electrical properties.

DESCRIPTION OF DRAWING(S) - The figure shows the ball grid array package with stiffener.

openings (114a,114c)

stiffener (600)

planar top surface (602)

planar bottom surface (604)

recesses step portions (606a,606c)

pp; 25 DwgNo 7/10

Title Terms: STIFFEN; BALL; GRID; ARRAY; PACKAGE; OPEN; RECESS; STEP; REGION; PLANE; TOP; SURFACE

Derwent Class: U11



International Patent Class (Main): H01L-023/10; H01L-023/498  
International Patent Class (Additional): H01L-023/13  
File Segment: EPI  
Manual Codes (EPI/S-X): U11-D01A3; U11-D01A5; U11-E02A3

13/9/10 (Item 10 from file: 350)  
DIALOG(R) File 350:Derwent WPIX  
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015558037 \*\*Image available\*\*

WPI Acc No: 2003-620193/200359

Related WPI Acc No: 2002-635363; 2002-635365; 2003-420004; 2003-678809;  
2003-678811; 2003-678812; 2003-720751; 2004-080035; 2004-080038;  
2004-080065; 2004-080066; 2004-256081; 2004-256082

XRPX Acc No: N03-494107

Ball grid array assembling method, involves connecting wire bond from  
bond pad of integrated circuit die to contact pad on substrate through  
opening in stiffener

Patent Assignee: BROADCOM CORP (BROA-N)

Inventor: KHAN R R ; ZHAO S Z

Number of Countries: 031 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1333490	A2	20030806	EP 20031957	A	20030130	200359 B

Priority Applications (No Type Date): US 2002284340 A 20021031; US  
2002352877 P 20020201

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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EP 1333490	A2	E	79	H01L-023/36	
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Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB  
GR HU IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR

Abstract (Basic): EP 1333490 A2

NOVELTY - The method involves mounting an integrated circuit (IC) die (102) in a centrally located cavity of a planar top surface of a stiffener (112) and attaching the bottom surface of the stiffener to the top surface of a substrate (104). A wire bond (108) from a bond pad (118) of the IC die is connected to a contact pad (120) on the substrate through a yore opening (114) in the stiffener.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) stiffener for stiffening a substrate in ball grid array package;

(2) ball grid array package; and

(3) stiffener forming method.

USE - For assembling IC package e.g. ball grid array ( BGA ) package (claimed).

ADVANTAGE - Improves electrical performance and heat spreading property of the BGA package. Facilitates attachment of electronic devices to the bottom surface of the BGA package.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the die-up flex BGA package.

IC die (102)  
substrate (104)  
wire bond (108)  
stiffener (112)  
opening (114)  
bond pad (118)

contact pad (120)  
pp; 79 DwgNo 4/51  
Title Terms: BALL; GRID; ARRAY; ASSEMBLE; METHOD; CONNECT; WIRE; BOND; BOND  
; PAD; INTEGRATE; CIRCUIT; DIE; CONTACT; PAD; SUBSTRATE; THROUGH; OPEN;  
STIFFEN  
Derwent Class: U11  
International Patent Class (Main): H01L-023/36  
International Patent Class (Additional): H01L-021/50; H01L-023/13  
File Segment: EPI  
Manual Codes (EPI/S-X): U11-D01A3; U11-D03B1; U11-E01A; U11-E02A3

13/9/11 (Item 11 from file: 350)  
DIALOG(R) File 350:Derwent WPIX  
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015359066 \*\*Image available\*\*  
WPI Acc No: 2003-420004/200339  
Related WPI Acc No: 2002-635363; 2002-635365; 2003-620193; 2003-678809;  
2003-678811; 2003-678812; 2003-720751; 2004-080035; 2004-080038;  
2004-080065; 2004-080066; 2004-256081; 2004-256082  
XRPX Acc No: N03-335381  
Ball grid array package for application specific integrated circuit,  
includes heat spreader arranged in contact with bonding agent to  
support circuit board and bonding agent distribution area is lower than  
that of substrate  
Patent Assignee: BROADCOM CORP (BROA-N)  
Inventor: KHAN R R ; ZHAO S Z  
Number of Countries: 032 Number of Patents: 002  
Patent Family:  
Patent No Kind Date Applicat No Kind Date Week  
US 20030057550 A1 20030327 US 2000742366 A 20001222 200339 B  
US 2001984259 A 20011029  
US 2002352877 P 20020201  
US 2002284312 A 20021031  
EP 1333491 A2 20030806 EP 20031959 A 20030130 200353  
Priority Applications (No Type Date): US 2002352877 P 20020201; US  
2000742366 A 20001222; US 2001984259 A 20011029; US 2002284312 A 20021031  
Patent Details:  
Patent No Kind Lan Pg Main IPC Filing Notes  
US 20030057550 A1 91 H01L-023/48 CIP of application US 2000742366  
CIP of application US 2001984259  
Provisional application US 2002352877  
EP 1333491 A2 E H01L-023/36  
Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB  
GR HU IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR

Abstract (Basic): US 20030057550 A1

NOVELTY - The bonding agent (112) is applied onto the surface of a  
substrate (104) for an area lower than that of the substrate area. The  
circuit board is attached to the heat spreader (402) maintained in  
contact with the bonding agent. The integrated circuit die mounted on  
the stiffener is enclosed by the epoxy resin.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for  
assembling method of ball grid array package.

USE - Ball grid array ( BGA ) package e.g. plastic/ceramic/tape  
BGA package for application specific integrated circuits (ASIC) and  
microprocessors.

ADVANTAGE - Releases thermal stress generated across die due to  
formation of die over heat spreader , thereby the damage of circuit

components is eliminated.

DESCRIPTION OF DRAWING(S) - The figure illustrates a cross sectional view of a die-up flex BGA package with heat spreader .

substrate (104)

bonding agent (112)

heat spreader (402)

pp; 91 DwgNo 4/56

Title Terms: BALL; GRID; ARRAY; PACKAGE; APPLY; SPECIFIC; INTEGRATE;  
CIRCUIT; HEAT ; SPREAD ; ARRANGE; CONTACT; BOND; AGENT; SUPPORT;  
CIRCUIT; BOARD; BOND; AGENT; DISTRIBUTE; AREA; LOWER; SUBSTRATE

Derwent Class: U11; V04

International Patent Class (Main): H01L-023/36; H01L-023/48

File Segment: EPI

Manual Codes (EPI/S-X): U11-D01A3; U11-D02B1; V04-T03

13/9/12 (Item 12 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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015041624 \*\*Image available\*\*

WPI Acc No: 2003-102140/200309

XRAM Acc No: C03-025610

XRFX Acc No: N03-081560

Ball grid array package to package and interface integrated circuit die with printed circuit board, has stiffener/ heat spreader , substrate with window-shaped aperture, integrated circuit die, and drop-in heat spreader

Patent Assignee: BROADCOM CORP (BROA-N)

Inventor: KHAN R R ; ZHAO S Z

Number of Countries: 102 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020109226	A1	20020815	US 2001783034	A	20010215	200309 B
WO 200267321	A2	20020829	WO 2002US2207	A	20020125	200309
EP 1374305	A2	20040102	EP 2002702083	A	20020125	200409
			WO 2002US2207	A	20020125	
TW 560019	A	20031101	TW 2002101690	A	20020131	200425
AU 2002235468	A1	20020904	AU 2002235468	A	20020125	200427

Priority Applications (No Type Date): US 2001783034 A 20010215

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

US 20020109226 A1 16 H01L-021/44

WO 200267321 A2 E H01L-023/00

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA  
CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN  
IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ  
OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA  
ZM ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR  
IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

EP 1374305 A2 E H01L-023/498 Based on patent WO 200267321

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT  
LI LT LU LV MC MK NL PT RO SE SI TR

TW 560019 A H01L-023/28

AU 2002235468 A1 H01L-023/00 Based on patent WO 200267321

Abstract (Basic): US 20020109226 A1

NOVELTY - A ball grid array package comprises a stiffener/ heat

**spreader** , a substrate with a central window-shaped aperture extending through the substrate, an integrated circuit die mounted to accessible portion of the stiffener/ **heat spreader** , and a drop-in **heat spreader** having a surface mounted to the second IC die surface.

DETAILED DESCRIPTION - A **ball grid** array package comprises a stiffener/ **heat spreader** , a substrate (104) having a central window-shaped aperture (112) extending through the substrate from its first surface to second surface, an integrated circuit (IC) die (102) mounted to an accessible portion of the stiffener/ **heat spreader** , and a drop-in **heat spreader** having a surface mounted to the second IC die surface. The first substrate surface is attached to a surface of the stiffener (110)/ **heat spreader** . A portion of the stiffener/ **heat spreader** is accessible through the central window-shaped aperture.

INDEPENDENT CLAIMS are included for the following:

- (a) a method of assembling a **ball grid** array package; and
- (b) a system for assembling a **ball grid** array package.

USE - To package and interface an integrated circuit die (preferably high speed ICs) with a printed circuit board.

ADVANTAGE - The invention has improved **heat spreading** capabilities and reduces **thermal** stress during the assembly processes, thus improving packaging yields. It also has an improved mechanical, **thermal** , and electrical performance.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a **ball grid** array package.

Die (102)  
Substrate (104)  
Window-shaped aperture (112)  
Epoxy (134, 204)  
pp; 16 DwgNo 2A/6

#### Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: Solder balls are attached to the second substrate surface. The drop-in **heat spreader** dissipates **heat** generated by the IC die. The second IC die surface includes a contact pad. A wire bond couples the contact pad to the drop-in **heat spreader** . A second surface of the drop-in **heat spreader** is attached to a printed circuit board. The drop-in **heat spreader** has a ridge around at least a portion of its circumference so that an area of the first planar drop-in **heat spreader** surface is greater than that of the second planar drop-in **heat spreader** surface. The IC die is mounted to the stiffener/ **heat spreader** with a first epoxy and the drop-in **heat spreader** is mounted to the IC die with a second epoxy (134, 204). The substrate is a tape substrate. The stiffener/ **heat spreader** and drop-in **heat spreader** have the same **thermal** expansion coefficient.

Title Terms: BALL; GRID; ARRAY; PACKAGE; PACKAGE; INTERFACE; INTEGRATE; CIRCUIT; DIE; PRINT; CIRCUIT; BOARD; STIFFEN; **HEAT** ; **SPREAD** ; SUBSTRATE ; WINDOW; SHAPE; APERTURE; INTEGRATE; CIRCUIT; DIE; DROP; **HEAT** ; **SPREAD**

Derwent Class: A85; L03; U11; V04; X24

International Patent Class (Main): H01L-021/44; H01L-023/00; H01L-023/28; H01L-023/498

International Patent Class (Additional): H01L-021/48; H01L-021/50; H01L-023/10; H01L-023/52; H01L-029/40

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A12-E07C; L04-C21; L04-C25

Manual Codes (EPI/S-X): U11-D01A3; U11-D01A5; U11-D01C6; U11-D02B1; U11-E02A3; V04-R04A; X24-A01C

Polymer Indexing (PS):

<01>

\*001\* 018; P0464-R D01 D22 D42 F47

\*002\* 018; Q9999 Q7454 Q7330; Q9999 Q7476 Q7330; ND01; Q9999 Q6644-R;  
K9416; K9483-R; K9676-R

13/9/13 (Item 13 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
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014922223 \*\*Image available\*\*  
WPI Acc No: 2002-742930/200281  
XRPX Acc No: N02-585290

Ball grid array package used for IC packaging, has heat spreader  
attached to substrate and several solder balls attached to the substrate  
outside the outer dimensional profile of the heat spreader

Patent Assignee: BROADCOM CORP (BROA-N)

Inventor: KHAN R R ; ZHANG T

Number of Countries: 027 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1256980	A2	20021113	EP 2002252969	A	20020426	200281 B
US 20020171144	A1	20021121	US 2001849537	A	20010507	200301

Priority Applications (No Type Date): US 2001849537 A 20010507

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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EP 1256980	A2	E	17	H01L-023/36	
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Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT  
LI LT LU LV MC MK NL PT RO SE SI TR

US 20020171144	A1	H01L-023/52
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Abstract (Basic): EP 1256980 A2

NOVELTY - Ball grid array ( BGA ) package has a substrate (104)  
with a first and second surface, and a heat spreader (504) with  
first and second surface. The first surface of the heat spreader is  
attached to the second surface of the substrate. Several solder balls  
(106) are attached to the second substrate surface outside the outer  
dimensional profile of the heat spreader .

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a  
method of assembling a ball grid array package.

USE - Used for integrated circuit packaging.

ADVANTAGE - Provides a BGA package which has improved heat  
spreading capabilities and higher levels of IC electrical performance.

DESCRIPTION OF DRAWING(S) - The drawing illustrates a cross  
sectional view of a die up BGA package with heat spreader .  
substrate (104)

heat spreader (504)

solder balls (106)

pp; 17 DwgNo 5/14

Title Terms: BALL; GRID; ARRAY; PACKAGE; IC; PACKAGE; HEAT ; SPREAD ;  
ATTACH; SUBSTRATE; SOLDER; BALL; ATTACH; SUBSTRATE; OUTER; DIMENSION;  
PROFILE; HEAT ; SPREAD

Derwent Class: U11

International Patent Class (Main): H01L-023/36; H01L-023/52

International Patent Class (Additional): H01L-023/367; H01L-023/48;  
H01L-023/498

File Segment: EPI

Manual Codes (EPI/S-X): U11-D01A3; U11-D01A5; U11-D01C6; U11-D02B1;  
U11-D03B3

13/9/14 (Item 14 from file: 350)  
DIALOG(R) File 350:Derwent WPIX  
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014814659 \*\*Image available\*\*

WPI Acc No: 2002-635365/200268

Related WPI Acc No: 2002-635363; 2003-420004; 2003-620193; 2003-678809;  
2003-678811; 2003-678812; 2003-720751; 2004-080035; 2004-080038;  
2004-080065; 2004-080066; 2004-256081; 2004-256082

XRAM Acc No: C02-179222

XRFX Acc No: N02-501902

Ball grid array package for integrated circuit devices, has  
substrate, stiffener, integrated circuit die, heat spreader, and  
solder balls

Patent Assignee: BROADCOM CORP (BROA-N); BACHER B (BACH-I); KHAN R R  
(KHAN-I); ZHAO S Z (ZHAO-I)

Inventor: BACHER B; KHAN R R; ZHAO S Z

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020079572	A1	20020627	US 2000742366	A	20001222	200268 B
TW 517359	A	20030111	TW 2001129877	A	20011203	200356

Priority Applications (No Type Date): US 2000742366 A 20001222; US  
2001984259 A 20011029

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
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US 20020079572	A1	36	H01L-023/10	
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TW 517359	A		H01L-023/28	
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Abstract (Basic): US 20020079572 A1

NOVELTY - A ball grid array package comprises a substrate with  
first and second surfaces; a stiffener having first and second  
surfaces; an integrated circuit die having first and second surfaces; a  
heat spreader having a first surface mounted to the second die  
surface; and solder balls attached to the second substrate surface.

DETAILED DESCRIPTION - A ball grid array (BGA) package  
comprises a substrate (104) having first and second surfaces; a  
stiffener (112) having a first surface and a second surface attached to  
the first substrate surface; an integrated circuit (IC) die (102)  
having a first surface mounted to the first stiffener surface and a  
second surface; a heat spreader (402) having a first surface  
mounted to the second IC die surface; and solder balls (106) attached  
to the second substrate surface. An INDEPENDENT CLAIM is included for a  
method of assembling the BGA package, comprising providing a tape  
substrate; attaching the first stiffener surface to the first substrate  
surface; mounting the IC die to the second stiffener surface; mounting  
the heat spreader to the IC die; and attaching the solder balls to  
the second substrate surface.

USE - For packaging integrated circuit devices.

ADVANTAGE - The inventive package has enhanced electrical and  
thermal characteristics, preferably improved heat spreading  
capabilities while also providing for high levels of IC electrical  
performance.

DESCRIPTION OF DRAWING(S) - The figure illustrates a  
cross-sectional view of a die-up flex BGA package.

Integrated circuit die (102)

Substrate (104)

Solder balls (106)

Wire bond (108)

Stiffener (112)  
Contact pad (118)  
**Heat spreader** (402)  
pp; 36 DwgNo 4/21

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The **heat spreader** is configured to dissipate **heat** generated by the IC die. It is configured to mount to the center of the second IC die surface. The IC die is mounted to the first stiffener surface with an epoxy, preferably a silver filled epoxy. The package includes an exposed first surface. The **heat spreader** has a second surface that forms a portion of the exposed first surface of the package. It is internal to the BGA package. The solder balls are located outside an outer dimensional profile of the IC die. Each solder ball is coupled to the stiffener through a corresponding via extending through the substrate. At least one solder ball is coupled to a first potential. The second IC die surface includes a contact pad (118). A wire bond (108) couples the corresponding contact pad to the second stiffener surface. The substrate includes a metal layer coupled to a second potential. The stiffener has opening(s) extending from the first stiffener surface to the second stiffener surface. The second IC die surface includes a second contact pad. A second wire bond couples the corresponding second contact pad to the metal layer by extending through the opening(s) in the stiffener. It connects to a corresponding second via that extends through the substrate. A metal ring is attached to the first stiffener surface, and improves **heat** dissipation from the stiffener. The substrate is a tape substrate or an organic substrate. Stud(s) corresponds to a wire bond opening in the stiffener, and bridges the stiffener across the corresponding wire bond opening. Preferred Property: An area of the second IC die surface is greater than an area of the first **heat spreader** surface.

Title Terms: BALL; GRID; ARRAY; PACKAGE; INTEGRATE; CIRCUIT; DEVICE;  
SUBSTRATE; STIFFEN; INTEGRATE; CIRCUIT; DIE; **HEAT** ; **SPREAD** ; SOLDER;  
BALL

Derwent Class: A85; L03; U11; V04

International Patent Class (Main): H01L-023/10; H01L-023/28

International Patent Class (Additional): H01L-021/56; H01L-023/34

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A99-A; L04-C17A

Manual Codes (EPI/S-X): U11-D01A3; U11-D01A5; U11-D01C6; U11-D02B1;

U11-E02A3

13/9/15 (Item 15 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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014814657 \*\*Image available\*\*

WPI Acc No: 2002-635363/200268

Related WPI Acc No: 2002-635365; 2003-420004; 2003-620193; 2003-678809;

2003-678811; 2003-678812; 2003-720751; 2004-080035; 2004-080038;

2004-080065; 2004-080066; 2004-256081; 2004-256082

XRPX Acc No: N02-501900

**Enhanced die-up BGA package has thermal connector with first surface coupled to metal plane of substrate and second surface coupled to printed circuit board**

Patent Assignee: BROADCOM CORP (BROA-N)

Inventor: BACHER B; **KHAN R R** ; ZHAO S Z

Number of Countries: 101 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020079562	A1	20020627	US 2000742366	A	20001222	200268 B
			US 2001984259	A	20011029	
WO 200252645	A2	20020704	WO 2001US44952	A	20011130	200268
TW 517359	A	20030111	TW 2001129877	A	20011203	200356
EP 1356516	A2	20031029	EP 2001272468	A	20011130	200379
			WO 2001US44952	A	20011130	
AU 2002217986	A1	20020708	AU 2002217986	A	20011130	200427

Priority Applications (No Type Date): US 2001984259 A 20011029; US 2000742366 A 20001222

#### Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020079562	A1		49	H01L-023/02	CIP of application US 2000742366
WO 200252645	A2	E		H01L-023/498	
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZM ZW					
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW					
TW 517359	A			H01L-023/28	
EP 1356516	A2	E		H01L-023/498	Based on patent WO 200252645
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
AU 2002217986	A1			H01L-023/498	Based on patent WO 200252645

#### Abstract (Basic): US 20020079562 A1

NOVELTY - An IC die (102) is mounted to the first surface of a substrate (104). Solder balls (106) are attached to corresponding exposed contact pads provided to the second surface of the substrate. The first surface of a **thermal** connector is coupled to the exposed metal plane provided to the second surface of the substrate. The second surface of the **thermal** connector is configured to be coupled to a printed circuit board.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for an assembling method of a **BGA** package.

USE - Enhanced die-up **BGA** package.

ADVANTAGE - Provides **BGA** package with improved **heat** dissipating capabilities, while also providing for high levels of IC electrical performance.

DESCRIPTION OF DRAWING(S) - The figure illustrates a cross-sectional view of a die-up flex **BGA** package with **heat spreader**.

IC die (102)

Substrate (104)

Solder balls (106)

pp; 49 DwgNo 4/36

Title Terms: ENHANCE; DIE; UP; PACKAGE; **THERMAL**; CONNECT; FIRST; SURFACE; COUPLE; METAL; PLANE; SUBSTRATE; SECOND; SURFACE; COUPLE; PRINT; CIRCUIT; BOARD

Derwent Class: A85; L03; U11; V04

International Patent Class (Main): H01L-023/02; H01L-023/28; H01L-023/498

International Patent Class (Additional): H01L-021/56; H01L-023/367;

H01L-023/50

File Segment: CPI; EPI

Manual Codes (EPI/S-X): U11-D01A3; U11-D01A5; V04-T03

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18/9/1 (Item 1 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
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016043649 \*\*Image available\*\*  
WPI Acc No: 2004-201500/200419  
XRAM Acc No: C04-079639  
XRPX Acc No: N04-160057

High power ball grid array includes an insulating layer of high thermal conductivity between a semiconductor chip and heat spreader  
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU ); SAMSUNG ELECTRONICS CO (SMSU )

Inventor: CHO T J; KIM M H; KWON H G; CHO T; KIM M; KWON H  
Number of Countries: 003 Number of Patents: 003  
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20040012928	A1	20040122	US 2003459400	A	20030610	200419 B
JP 2004023103	A	20040122	JP 2003167601	A	20030612	200419
KR 2003096461	A	20031231	KR 200232972	A	20020612	200426

Priority Applications (No Type Date): KR 200232972 A 20020612

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040012928	A1		10	H05K-007/20	
JP 2004023103	A		12	H01L-023/12	
KR 2003096461	A			H01L-023/36	

Abstract (Basic): US 20040012928 A1

NOVELTY - High power ball grid array includes an insulating layer of high thermal conductivity between a semiconductor chip and heat spreader .

DETAILED DESCRIPTION - A high power ball grid array comprises:  
(a) a printed circuit board having a through hole;  
(b) connection pads on a bottom surface of the printed circuit board proximate the through hole;

(c) solder balls (210) on the bottom surface of the printed circuit board proximate the through hole and the connection pads;

(d) heat spreader on a top surface of the printed circuit board and over the through hole, where the heat spreader includes an insulating layer of a high thermal conductivity;

(e) semiconductor chip (101) mounted on the bottom surface of the heat spreader inside the through hole, where the semiconductor chip includes contact pads (201), each contact pad electrically connected to a corresponding connection pad; and

(f) passive film (230) filling the through hole and surrounding the semiconductor chip.

INDEPENDENT CLAIMS are also included for the following:

(a) a method for manufacturing a heat spreader comprising: forming first and second metal layers on first and second surfaces of an insulating layer (111); forming a region configured to attach to a semiconductor chip by patterning the first metal layer; cutting a first groove through the first metal layer to a first predetermined depth of the insulating layer; cutting a second groove through the second metal layer to a second predetermined depth of the insulating layer, where the first and second grooves are aligned; and forming a protection layer (115) on the first and second metal layers; and

(b) a heat spreader comprising: a heat -emitting board that is formed by sequentially depositing a supporting ceramic layer having a board shape, a heat-emitting metal layer, and a protection layer; and a

lower metal layer (120) formed on a bottom surface of the supporting ceramic layer.

USE - Used as high power ball grid array.

ADVANTAGE - By interposing a ceramic insulating layer between semiconductor chip and heat spreader, charge generation between semiconductor chip and heat spreader is reduced, and defects such as electrostatic discharge is reduced during testing and mounting of the package.

DESCRIPTION OF DRAWING(S) - The figure is a sectional view of a high-power BGA package.

Semiconductor chip (101)

Heat spreader (110)

Insulating layer (111)

Protection layer (115)

Lower metal layer (120)

Black oxide layer (140)

Printed circuit board (200)

Contact pads (201)

Dam (203)

Solder balls (210)

Passive film (230)

pp; 10 DwgNo 1/12

#### Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: A dam (203) surrounds the through hole and extrudes from the bottom surface of the printed circuit board.

POLYMERS - Preferred Materials: The printed circuit board comprises material(s) consisting of synthetic resin.

CERAMICS AND GLASS - Preferred Materials: The printed circuit board comprises material(s) consisting of ceramic. The insulating layer consists of aluminum nitride (AlN), beryllium oxide (BeO), or aluminum oxide (Al<sub>2</sub>O<sub>3</sub>).

METALLURGY - Preferred Materials: The first and second metal layers consist of copper or copper alloy. The protection layer comprises nickel or nickel alloy.

Preferred Method: The first and second metal layers are adhered to corresponding surface of the insulating layer by direct copper bonding, or metal brazing. The first and second metal layers are formed by forming a photoresist on the first metal layer, forming a mask pattern of the region by applying a photoprocess to the photoresist, and transferring the mask pattern onto the first metal layer by etching the first metal layer exposed by the mask pattern. The etching is performed by wet etching using an acid solution. The protection layer is formed by electrolysis plating. The cutting step is performed using a laser. The step of forming a region comprises forming a black oxide layer (140) for a junction on the surface of the first metal layer where the region is formed.

Title Terms: HIGH; POWER; BALL; GRID; ARRAY; INSULATE; LAYER; HIGH; THERMAL ; CONDUCTING; SEMICONDUCTOR ; CHIP; HEAT; SPREAD

Derwent Class: L03; U11; V04

International Patent Class (Main): H01L-023/12; H01L-023/36; H05K-007/20

International Patent Class (Additional): H01L-023/15; H01L-023/373

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L04-C25

Manual Codes (EPI/S-X): U11-D01A3; U11-D01A5; U11-D02B; V04-T03A

18/9/2 (Item 2 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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015960222      \*\*Image available\*\*  
WPI Acc No: 2004-118063/200412  
Related WPI Acc No: 2003-898552  
XRAM Acc No: C04-047338  
XRPX Acc No: N04-094270

Application of heat spreader in semiconductor package, e.g. quad flat package, comprises providing heat spreader having two surfaces for semiconductor package, heat spreader being provided with groove(s) across heat spreader

Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)

Inventor: CHEN K; TSAO P; WANG J

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6607942	B1	20030819	US 2001912739	A	20010726	200412 B

Priority Applications (No Type Date): US 2001912739 A 20010726

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 6607942	B1	9	H01L-021/48	

Abstract (Basic): US 6607942 B1

NOVELTY - A heat spreader is applied in a semiconductor package by providing a heat spreader (40) having two surfaces for a semiconductor package, the heat spreader being provided with a groove(s) (42) across the heat spreader .

DETAILED DESCRIPTION - The application of a heat spreader in a semiconductor package comprises providing a semiconductor die (12); providing a substrate (10) over the surface of which the semiconductor device is to be mounted; providing a stiffener (23) for the semiconductor package; mounting the semiconductor device over the substrate , providing an adhesive interface for the stiffener, placing the stiffener in position and establishing electrical contact between the semiconductor device and the substrate ; providing a heat spreader having two surfaces for a semiconductor package, the heat spreader being provided with a groove(s) across the heat spreader ; providing an adhesive interface for the heat spreader ; and placing the heat spreader over the adhesive interface to allow direct physical with die, thus reducing the stress on solder ball (26) connections between the semiconductor die and the substrate .

An INDEPENDENT CLAIM is also included for creating a semiconductor package, comprising providing a semiconductor device mounting support having two surfaces , first points of electrical contact being provided in the first surface of the semiconductor device mounting support, second points of electrical contact being provided in the second surface , layer(s) of interconnected lines being provided in the semiconductor device mounting support on the two surfaces of the semiconductor device mounting support; providing a semiconductor device being provided with points of electrical contact in a first surface of the semiconductor device; positioning the semiconductor device above the second surface of the semiconductor device mounting support, the first surface of the semiconductor device facing the second surface of the semiconductor device mounting support, aligning and establishing contact between the points of electrical contact provided in the first surface , of the semiconductor device and the points of electrical contact provided in the second surface of the semiconductor device mounting support; establishing electrical continuity between the points of electrical contact provided in the first surface of the

semiconductor device, and the points of electrical contact provided in the second surface of the semiconductor device mounting support by a reflow of the points of electrical contact provided in the first surface of the semiconductor device; providing an underfill (13) for the semiconductor device, leaving a second surface of the semiconductor device exposed; applying a first adhesive layer over the second surface area of the semiconductor device mounting support that is not being covered by the underfill; providing a semiconductor device stiffener having two surfaces, the stiffener being provided with an opening penetrating from the first to the second surface of the stiffener, and of size for insertion of the semiconductor device; positioning the stiffener over the first adhesive layer applied over the second surface of the semiconductor device mounting support, the first surface of the stiffener facing the first adhesive layer, the opening provided in the stiffener being aligned with the semiconductor device mounted on the second surface of the semiconductor device mounting support; applying a second adhesive layer over the second surface of the semiconductor device and the second surface of the stiffener; providing a heat spreader; positioning the first surface of the heat spreader over the surface of the second adhesive layer; providing the first surface of the semiconductor device mounting support with a solder mask, openings in the solder mask exposing the contact points provided in the first surface of the semiconductor device mounting support; inserting solder balls into the openings provided in the solder mask; and establishing electrical continuity between the solder balls inserted in the openings in the solder mask, and the contact points provided in the first surface of the semiconductor device mounting support by a process of reflow.

USE - Used for the application of a heat spreader in a semiconductor package, e.g. quad flat package or ball grid array package.

ADVANTAGE - The division of the heat spreader results in a reduction of the mechanical and thermal stress that is introduced by the heat spreader, into the device package.

DESCRIPTION OF DRAWING(S) - The figures show a cross section of the semiconductor package, and a top view of a heat spreader.

Substrate (10)  
Semiconductor die (12)  
Underfill (13)  
Stiffener (23)  
Solder ball (26)  
Heat spreader (40)  
Groove (42)

pp; 9 DwgNo 4a, 4c/4

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The heat spreader is a rectangular cube having parallel two surfaces of equal surface area bounded by four interconnecting surfaces, a surface area of the interconnecting surfaces being smaller than the surface area of the two surfaces by an amount, the first surface of the heat spreader facing the semiconductor die after mounting the die in the semiconductor package of which the heat spreader is an integral part. The groove(s) comprises two intersecting grooves provided at distances from side boundaries of the first surface. The groove(s) is provided using etching or machining or punching of the first surface of the heat spreader. Preferred Material: The semiconductor device mounting support is a printed circuit board, a metallized structure, or a glass substrate.

Title Terms: APPLY; HEAT; SPREAD; **SEMICONDUCTOR** ; PACKAGE; QUAD; FLAT;  
PACKAGE; COMPRISE; HEAT; SPREAD; TWO; SURFACE; **SEMICONDUCTOR** ; PACKAGE;  
HEAT; SPREAD; GROOVE; HEAT; SPREAD

Derwent Class: L03; V04

International Patent Class (Main): H01L-021/48

International Patent Class (Additional): H01L-023/34

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L04-C25

Manual Codes (EPI/S-X): V04-T03A

18/9/3 (Item 3 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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015595699 \*\*Image available\*\*

WPI Acc No: 2003-657854/200362

Related WPI Acc No: 2001-136529; 2002-162985; 2003-531024; 2003-576564

XRAM Acc No: C03-179620

XRPX Acc No: N03-524210

**Assembling chip scale package involves attaching opposing second  
surface of semiconductor die to paddle and disconnecting the paddle  
having the semiconductor die from the metallic paddle frame**

Patent Assignee: CORISIS D J (CORI-I); MICRON TECHNOLOGY INC (MICR-N)

Inventor: CORISIS D J; CORISIS D J

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030084566	A1	20030508	US 9828134	A	19980223	200362 B
			US 99342788	A	19990629	
			US 2000679940	A	20001004	
			US 2002315527	A	20021209	
US 6735859	B2	20040518	US 9828134	A	19980223	200433
			US 99342788	A	19990629	
			US 2000679940	A	20001004	
			US 2002315527	A	20021209	

Priority Applications (No Type Date): US 9828134 A 19980223; US 99342788 A  
19990629; US 2000679940 A 20001004; US 2002315527 A 20021209

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030084566	A1		8	H05K-013/00	Div ex application US 9828134 Cont of application US 99342788 Cont of application US 2000679940 Cont of patent US 6163956 Div ex patent US 6314639 Cont of patent US 6505400
US 6735859	B2			H01R-043/00	Div ex application US 9828134 Cont of application US 99342788 Cont of application US 2000679940 Cont of patent US 6163956 Div ex patent US 6314639 Cont of patent US 6505400

Abstract (Basic): US 20030084566 A1

NOVELTY - A chip scale package is assembled by:

(a) attaching the opposing **second surface** of the **semiconductor**  
die (20) to the paddle; and

(b) disconnecting the paddle having the **semiconductor** die from  
the metallic paddle frame. The paddle serves as a heat sink (52) for

the **semiconductor** die.

USE - Assembling a chip scale package.

ADVANTAGE - The process produces a high density **semiconductor** device with **heat spreader** /dissipater in easy and economic manner. The produced device has improved reliability.

DESCRIPTION OF DRAWING(S) - The drawing shows a side view of a circuit board, which has reversibly mounted paddle-bonded **semiconductor** die with **ball grid** arrays and with **heat spreading** chip scale package.

**Semiconductor** die (20)

**Substrate** (42)

Heat sink (52)

pp; 8 DwgNo 4/5

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The **semiconductor** die is tested for electrical properties while the paddle is located between the side rails of the metallic paddle frame. The bond pads of **semiconductor** die are connected to circuits of **printed circuit** board. The **semiconductor** die is attached to the paddle by an electrically non-conductive adhesive material. The opposing **second surface** of the **semiconductor** die is attached to the paddle by electrically conductive material. Conductive bumps are provided on the bond pads on the active surface of the **semiconductor** die for conductive **ball grid** array connection to the **substrate** (42). The bond pads on the active surface of the **semiconductor** die are connected by a conductive **ball grid** array connection to the circuits on the **substrate**.

Preferred Materials: The electrically conductive material comprises eutectic material including gold-silicon eutectic layer.

POLYMERS - Preferred Materials: The non-conductive material comprises polymer, preferably polyimide or epoxy. It can be polyimide tape. The electrically conductive material comprises a polymer filled with conductive particles

Title Terms: ASSEMBLE; CHIP; SCALE; PACKAGE; ATTACH; OPPOSED; SECOND; SURFACE; **SEMICONDUCTOR** ; DIE; PADDLE; DISCONNECT; PADDLE; **SEMICONDUCTOR** ; DIE; METALLIC; PADDLE; FRAME

Derwent Class: A85; L03; U11; V04

International Patent Class (Main): H01R-043/00; H05K-013/00

International Patent Class (Additional): H01H-001/00; H05K-003/34

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A12-E07C; L04-C25; L04-F01

Manual Codes (EPI/S-X): U11-D01A3; U11-D01A8; U11-D02B2; U11-E02A2;

U11-E02A3; V04-P; V04-R04A; V04-V

Polymer Indexing (PS):

<01>

\*001\* 018; P1081-R F72 D01; S9999 S1650 S1649

\*002\* 018; P0464-R D01 D22 D42 F47

\*003\* 018; ND07; Q9999 Q7454 Q7330; Q9999 Q7476 Q7330; N9999 N5721-R; Q9999 Q6644-R; B9999 B3270 B3190

<02>

\*001\* 018; P0000

\*002\* 018; ND07; Q9999 Q7454 Q7330; Q9999 Q7476 Q7330; N9999 N5721-R; K9449; B9999 B3269 B3190

\*003\* 018; A999 A237; S9999 S1456-R; B9999 B3269 B3190

18/9/4 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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015468878      **\*\*Image available\*\***

WPI Acc No: 2003-531024/200350

Related WPI Acc No: 2001-136529; 2002-162985; 2003-576564; 2003-657854

XRAM Acc No: C03-143258

XRPX Acc No: N03-421279

**Production of, e.g., flip-chip-on-board for connection to printed circuit board, by providing paddle frame having left and right side rails and paddle between the rails and attaching semiconductor die to the paddle**

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)

Inventor: CORISIS D J

Number of Countries: 001    Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6505400	B1	20030114	US 9828134	A	19980223	200350 B
			US 99342788	A	19990629	
			US 2000679940	A	20001004	

Priority Applications (No Type Date): US 9828134 A 19980223; US 99342788 A 19990629; US 2000679940 A 20001004

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6505400	B1		8	H05K-003/30	Div ex application US 9828134 Cont of application US 99342788 Cont of patent US 6163956 Div ex patent US 6314639

Abstract (Basic): US 6505400 B1

NOVELTY - A **semiconductor** device assembly is produced by: providing **semiconductor** die having bond pads on its active surface, a metallic paddle frame having paddle between its side rails for receiving the **semiconductor** die, and a conductive projection on each bond pad for connection to a **substrate** ; attaching the **semiconductor** die to the paddle; and disconnecting the paddle from the paddle frame.

DETAILED DESCRIPTION - Production of **semiconductor** device assembly involves: providing a **semiconductor** die (20) having an active **surface** with bond pads (32) and an opposing **second surface** , a metallic paddle frame (12) having paddle (22) between its left and right side rails (14, 16) for receiving the **semiconductor** die, and a conductive projection on each bond pad for connection to **substrate** ; attaching the **second surface** of the **semiconductor** die to the paddle; and disconnecting the paddle with attached **semiconductor** die from the metallic paddle frame.

USE - The method is for assembling a **semiconductor** device, e.g. flip-chip-on-board for connection to the **substrate** , i.e. **printed circuit board** (claimed).

ADVANTAGE - The invented method produces improved and high-density **semiconductor** assemblies with enhanced reliability, ease of production, and reduced production costs. Current methods of lead frame production may be used to produce the paddle frame metal strip. The **heat sink/ spreader** /dissipater provides better temperature control and increased reliability of the assembly. No additional specially-designed equipment is required.

DESCRIPTION OF DRAWING(S) - The figure is a plan view of a paddle frame and attached **semiconductor** dice.

Paddle frame (12)  
Side rails (14, 16)  
**Semiconductor** die (20)  
Paddle (22)  
Bond pads (32)

pp; 8 DwgNo 1/5

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The method also involves testing electrical properties of **semiconductor** die while the paddle is between the side rails. The bond pads are connected to the circuits of the **printed circuit** board. The **semiconductor** die is attached to the paddle by non-conductive adhesive material. The second end of **semiconductor** die is attached to the paddle by a conductive material. The method also involves providing conductive bumps on the bond pads of the **semiconductor** die for conductive **ball - grid -array** connection to the **substrate** .

POLYMERS - Preferred Material: The non-conductive material comprises polymer, polyimide, epoxy, or polyimide tape. The conductive material may be a polymer filled with conductive particles.

INORGANIC CHEMISTRY - Preferred Material: The conductive material is a gold-silicon eutectic layer

Title Terms: PRODUCE; FLIP; CHIP; BOARD; CONNECT; PRINT; CIRCUIT; BOARD; PADDLE; FRAME; LEFT; RIGHT; SIDE; RAIL; PADDLE; RAIL; ATTACH; **SEMICONDUCTOR** ; DIE; PADDLE

Derwent Class: A85; L03; S01; U11; V04

International Patent Class (Main): H05K-003/30

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A12-E07A; A12-E07C; L03-H04E; L04-F01

Manual Codes (EPI/S-X): S01-G02B1; U11-D01A3; U11-D01C6; U11-D02B1;

U11-E01C; V04-R04B

Polymer Indexing (PS):

<01>

\*001\* 018; P1081-R F72 D01

\*002\* 018; ND01; K9676-R; K9483-R; K9574 K9483; Q9999 Q7476 Q7330; K9416

\*003\* 018; Q9999 Q6644-R; B9999 B3270 B3190

\*004\* 018; Q9999 Q6633

<02>

\*001\* 018; P0464-R D01 D22 D42 F47

\*002\* 018; ND01; K9676-R; K9483-R; K9574 K9483; Q9999 Q7476 Q7330; K9416

\*003\* 018; Q9999 Q6644-R; B9999 B3270 B3190

<03>

\*001\* 018; P0000

\*002\* 018; ND01; K9676-R; K9483-R; K9574 K9483; Q9999 Q7476 Q7330; K9416

\*003\* 018; B9999 B3269 B3190; K9449

\*004\* 018; D00 Si 4A Au 1B Tr; A999 A237; B9999 B3269 B3190; S9999  
S1456-R

?



22/9/1 (Item 1 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
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016207124 \*\*Image available\*\*

WPI Acc No: 2004-365010/200434

XRAM Acc No: C04-137808

XRPX Acc No: N04-291969

Multi-package module for, e.g. building computers, includes stacked lower  
and inverted upper packages that are interconnected by wire bonding

Patent Assignee: CHIPPAC INC (CHIP-N)

Inventor: KARNEZOS M; CARSON F

Number of Countries: 106 Number of Patents: 008

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200434433	A2	20040422	WO 2003US31987	A	20031008	200434 B
US 20040113253	A1	20040617	US 2002417277	P	20021008	200440
			US 2003460541	P	20030404	
			US 2003618933	A	20030714	
			US 2003681572	A	20031008	
US 20040113254	A1	20040617	US 2002417277	P	20021008	200440
			US 2003460541	P	20030404	
			US 2003618933	A	20030714	
			US 2003681583	A	20031008	
US 20040113255	A1	20040617	US 2002417277	P	20021008	200440
			US 2003460541	P	20030404	
			US 2003618933	A	20030714	
			US 2003681584	A	20031008	
US 20040113275	A1	20040617	US 2002417277	P	20021008	200440
			US 2003460541	P	20030404	
			US 2003618933	A	20030714	
			US 2003681747	A	20031008	
US 20040119152	A1	20040624	US 2002417277	P	20021008	200442
			US 2003460541	P	20030404	
			US 2003618933	A	20030714	
			US 2003681734	A	20031008	
US 20040119153	A1	20040624	US 2002417277	P	20021008	200442
			US 2003460541	P	20030404	
			US 2003618933	A	20030714	
			US 2003681735	A	20031008	
US 20040124518	A1	20040701	US 2002417277	P	20021008	200444
			US 2003460541	P	20030404	
			US 2003618933	A	20030714	
			US 2003681833	A	20031008	

Priority Applications (No Type Date): US 2003618933 A 20030714; US  
2002417277 P 20021008; US 2003460541 P 20030404; US 2003681572 A 20031008  
; US 2003681583 A 20031008; US 2003681584 A 20031008; US 2003681747 A  
20031008; US 2003681734 A 20031008; US 2003681735 A 20031008; US  
2003681833 A 20031008

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

WO 200434433 A2 E 95 H01L-000/00

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA  
CH CN CO CR CU CZ DE DK DM DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL  
IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NI  
NO NZ OM PG PH PL PT RO RU SC SD SE SG SK SL SY TJ TM TN TR TT TZ UA UG  
US UZ VC VN YU ZA ZM ZW

Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB  
GH GM GR HU IE IT KE LS LU MC MW MZ NL OA PT RO SD SE SI SK SL SZ TR TZ  
UG ZM ZW

US 20040113253 A1	H01L-023/02	Provisional application US 2002417277 Provisional application US 2003460541 CIP of application US 2003618933
US 20040113254 A1	H01L-023/538	Provisional application US 2002417277 Provisional application US 2003460541 CIP of application US 2003618933
US 20040113255 A1	H01L-023/538	Provisional application US 2002417277 Provisional application US 2003460541 CIP of application US 2003618933
US 20040113275 A1	H01L-023/02	Provisional application US 2002417277 Provisional application US 2003460541 CIP of application US 2003618933
US 20040119152 A1	H01L-023/538	Provisional application US 2002417277 Provisional application US 2003460541 CIP of application US 2003618933
US 20040119153 A1	H01L-023/538	Provisional application US 2002417277 Provisional application US 2003460541 CIP of application US 2003618933
US 20040124518 A1	H01L-021/48	Provisional application US 2002417277 Provisional application US 2003460541 CIP of application US 2003618933

Abstract (Basic): WO 200434433 A2

NOVELTY - A multi-package module comprises stacked lower and upper packages (400, 500) containing a die (414, 514) attached to a **substrate**. The upper package is inverted and the **substrates** (412, 512) are interconnected by wire bonding.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method for making a multipackage module comprising placing over the first package an inverted second package including at least one die on a second package **substrate**, and forming wire bond z-interconnects between the **substrates**.

USE - For building computers, portable telecommunications device, mobile communication devices, and consumer and industrial electronic devices (claimed).

ADVANTAGE - The invention provides excellent manufacturability, high design flexibility, and low cost stack package module having a low profile and small footprint.

DESCRIPTION OF DRAWING(S) - The figure shows a diagrammatic sketch in a sectional view of a multi-package module.

Lower and upper packages (400, 500)

**Substrates** (412, 512)

Die (414, 514)

Wire bond (416, 516)

Upper surface (419, 519)

pp; 95 DwgNo 5A/18

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: At least one package has wire bond (416, 516) interconnect of the die with the **substrate**. The package is fully encapsulated, a **ball grid array** package, a **land grid array** package, or **flip chip** interconnect of the die with the **substrate**. The upper package includes a **bump chip carrier type substrate**. The module further includes a **heat spreader**, an electromagnetic shield for at least one package, and a

third stacked package. The first package comprises an unsingulated strip of packages. A curable adhesive is applied on an upper surface (419, 519) of the first substrate. The second package is inverted and placed on the adhesive.

Title Terms: MULTI; PACKAGE; MODULE; BUILD; COMPUTER; STACK; LOWER; INVERT; UPPER; PACKAGE; INTERCONNECT; WIRE; BOND

Derwent Class: A85; L03; U11; W02

International Patent Class (Main): H01L-000/00; H01L-021/48; H01L-023/02; H01L-023/538

International Patent Class (Additional): H01L-023/52; H01L-023/552

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A11-B05; A12-E04; A12-E07C; L04-F01; L04-F03

Manual Codes (EPI/S-X): U11-D01A3; U11-D01A6; U11-D03A2; W02-G02A; W02-G02H

Polymer Indexing (PS):

<01>

\*001\* 2004; P0000

\*002\* 2004; ND01; ND07; Q9999 Q7523; Q9999 Q7476 Q7330; Q9999 Q7330-R; Q9999 Q9449 Q8173; B9999 B3623 B3554; B9999 B4035 B3930 B3838 B3747; K9483-R; N9999 N7170 N7023

<02>

\*001\* 2004; P0000

\*002\* 2004; ND01; ND07; Q9999 Q7523; Q9999 Q7476 Q7330; Q9999 Q7330-R; Q9999 Q9449 Q8173; B9999 B3623 B3554; B9999 B4035 B3930 B3838 B3747; K9483-R; B9999 B4988-R B4977 B4740; Q9999 Q6644-R; N9999 N7147 N7034 N7023

22/9/2 (Item 2 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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016009107 \*\*Image available\*\*

WPI Acc No: 2004-166958/200416

XRAM Acc No: C04-066131

XRPX Acc No: N04-133065

Semiconductor device, e.g. ball - grid -array package-type semiconductor device, comprises semiconductor die provided with standoffs on its surface

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)

Inventor: JAMES S L; WILLIAMS V M

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030201525	A1	20031030	US 2002132834	A	20020425	200416 B

Priority Applications (No Type Date): US 2002132834 A 20020425

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030201525	A1		25	H01L-021/44	

Abstract (Basic): US 20030201525 A1

NOVELTY - A semiconductor device, e.g. ball - grid -array package-type semiconductor device, comprises a semiconductor die (12a, 12b) mounted on a support substrate (14). Standoff(s) (16) is provided on first surface of semiconductor die.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(a) a semiconductor die package comprising a semiconductor device disposed within an encapsulating material (15);

(b) a mold tool for fabricating a semiconductor die package, comprising a molding chamber defined between a pair of molding plates,

with each molding plate having an inner surface provided with standoff having a height effective to contact a surface of a die positioned within the molding chamber and to restrict vertical movement of the die within the molding chamber during an encapsulation process;

(c) a method of fabricating a **semiconductor** device by providing a **substrate** and a **semiconductor** die, forming a standoff on **first surface** of the die, and mounting the **second surface** of the die on **first surface** of the **substrate** ; and

(d) a method of fabricating a **semiconductor** die package by positioning a die/ **substrate** unit within a molding chamber of a mold tool, and introducing molding compound into the molding chamber.

USE - For use as **ball - grid -array** package-type **semiconductor** device.

ADVANTAGE - The provision of standoffs facilitates formation of die package by preventing the tape **substrate** from bending during encapsulation.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional, side elevational view of an encapsulated die package.

**Semiconductor** die (12a, 12b)

Support **substrate** (14)

Encapsulating material (15)

Standoffs (16)

Conductive balls (26)

pp; 25 DwgNo 1/29

#### Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Parameters: When the die is positioned in a mold cavity between two mold plates, the height of the standoff is sufficient to maintain the die in centralized and planar orientation within the mold cavity during encapsulation process.

Preferred Components: The standoff is cylindrical, conical, square, rectangular, spherical, hemispherical, or tubular. It comprises graphic design, e.g. number, letter, and/or logo; a decal; or a pre-formed structure mounted on the die surface with an adhesive paste or double-sided adhesive tape. The standoff may be a dam including a heat sink disposed on die surface. A heat sink may be disposed on die **surface** adjacent the standoff. Conductive balls (26) are disposed on the **second surface** of die in a **ball grid** array. The conductive balls comprise solder, electrically conductive polymer, conductive epoxy, or conductor-filled epoxy.

Preferred Method: Formation of standoff includes screen-printing, stenciling, coating, masking, stamping, **heat** -stamping, spray coating, or direct **spreading** a material on die surface. The standoff may be formed by dispensing flowable material in the die using a liquid capillary, and allowing the flowable material to solidify. The standoff can also be formed by electroplating or anodizing process, or by injecting molding, extrusion, blow molding, compression molding, transfer molding, or thermoforming a plastic material.

METALLURGY - Preferred Materials: The standoff may be made of thermally conductive material, e.g. aluminum, gold, silver, or preferably copper foil.

POLYMERS - Preferred Materials: The standoff is made of flexible, thermoplastic or thermoset material, e.g. acrylic, polyamide, polyethylene terephthalate, polyethylene, polypropylene, polystyrene, polyvinyl chloride resin, polycarbonate, polyurethane, or Novolak epoxy resin. The support **substrate** is made of flexible polyimide tape, bismaleimide triazine resin, FR-4 laminate, FR-5 laminate, ceramic, metal-clad fiberboard, or metal leadframe.

Title Terms: **SEMICONDUCTOR** ; DEVICE; BALL; GRID; ARRAY; PACKAGE; TYPE;

**SEMICONDUCTOR** ; DEVICE; COMPRISE; **SEMICONDUCTOR** ; DIE; SURFACE

Derwent Class: A18; A28; A32; A92; L03; U11

International Patent Class (Main): H01L-021/44

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A12-E07C; L04-C20C

Manual Codes (EPI/S-X): U11-C05E

Polymer Indexing (PS):

<01>

\*001\* 2004; P1081-R F72 D01; S9999 S1650 S1649

\*002\* 2004; G2324 D01 D23 D22 D31 D76 D45 D50 D83 F19 F07-R; G0953 G0817  
D01 D23 D22 D41 D51 D54 D57 D59 D75 F72 E00 E01; P1105-R D01 F07;  
H0022 H0011

\*003\* 2004; B9999 B4035 B3930 B3838 B3747; N9999 N5798 N5787 N5765; N9999  
N7078-R N7034 N7023; N9999 N7067 N7034 N7023; N9999 N6484-R N6440;  
N9999 N5970-R; N9999 N6451 N6440; N9999 N6462 N6440; N9999 N6542  
N6440; N9999 N6111 N6097; B9999 B4035 B3930 B3838 B3747; Q9999  
Q7818-R

<02>

\*001\* 2004; P0088-R; H0317; H0328; S9999 S1434

\*002\* 2004; P0635-R F70 D01; H0317; H0328; S9999 S1434

\*003\* 2004; P0884 P1978 P0839 H0293 F41 D01 D11 D10 D19 D18 D31 D50 D63  
D76 D90 F90 E21 E00; H0317; H0328; S9999 S1434

\*004\* 2004; R00326 G0044 G0033 G0022 D01 D02 D12 D10 D51 D53 D58 D82;  
H0000; H0317; H0328; S9999 S1434; P1150 ; P1161

\*005\* 2004; R00964 G0044 G0033 G0022 D01 D02 D12 D10 D51 D53 D58 D83;  
H0000; H0317; H0328; S9999 S1434; P1150 ; P1343

\*006\* 2004; R00708 G0102 G0022 D01 D02 D12 D10 D19 D18 D31 D51 D53 D58  
D76 D88; H0000; H0317; H0328; S9999 S1434; P1741 ; P1752

\*007\* 2004; R00338 G0544 G0022 D01 D12 D10 D51 D53 D58 D69 D82 Cl 7A;  
H0000; H0317; H0328; S9999 S1434; P1796 P1809

\*008\* 2004; P0862 P0839 F41 F44 D01 D63; H0317; H0328; S9999 S1434

\*009\* 2004; P1592-R F77 D01; H0317; H0328; S9999 S1434

\*010\* 2004; P0464-R D01 D22 D42 F47; H0317; H0328; S9999 S1434

\*011\* 2004; B9999 B4035 B3930 B3838 B3747; N9999 N5798 N5787 N5765; N9999  
N7078-R N7034 N7023; N9999 N7067 N7034 N7023; N9999 N6484-R N6440;  
N9999 N5970-R; N9999 N6451 N6440; N9999 N6462 N6440; N9999 N6542  
N6440; N9999 N6111 N6097; ND07; ND01; Q9999 Q7476 Q7330; K9483-R

22/9/3 (Item 3 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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015948945 \*\*Image available\*\*

WPI Acc No: 2004-106786/200411

XRAM Acc No: C04-043494

XRPX Acc No: N04-084861

Multichip package comprises tape attached to first chip and includes  
conductive material layer, which is aluminum layer, copper layer and/or  
composite layer including copper layer and heat transfer improving layer  
formed on copper layer

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU )

Inventor: BAEK J H; KIM M H; LEE T G; LIM Y H; BAEK J; IM Y; KIM M; LEE T

Number of Countries: 003 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030210533	A1	20031113	US 2003410011	A	20030407	200411 B
JP 2003332524	A	20031121	JP 2003114660	A	20030418	200411
KR 2003087742	A	20031115	KR 200225626	A	20020509	200420

Priority Applications (No Type Date): KR 200225626 A 20020509

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

US 20030210533 A1 11 H05K-007/02  
JP 2003332524 A 8 H01L-025/065  
KR 2003087742 A H01L-023/12

Abstract (Basic): US 20030210533 A1

NOVELTY - A multichip package (100) comprises a tape (116) attached to a first chip (106) and includes a conductive material layer.

DETAILED DESCRIPTION - A multichip package (MCP) comprises:

(a) a package **substrate** (102) including bond fingers formed on a first set of its opposite sides;

(b) a first chip overlying the **substrate** and including first bond pads formed adjacent the bond fingers of the **substrate** ;

(c) a tape attached to the first chip and including a conductive material layer; and

(d) a second chip (120) attached to the tape and including second bond pads formed adjacent the bond fingers of the **substrate** .

The bond pads of the first and second chips are electrically connected to the bond fingers of the **substrate** .

USE - Used to produce miniaturized and lightweight electronic products.

ADVANTAGE - Improved **heat spread** characteristics in which **heat** generated in a chip is not trapped and is smoothly **spread** so the **thermal** performance of the MCP is improved.

DESCRIPTION OF DRAWING(S) - The figure is a cross-section explaining the effect of MCP.

Multichip package (100)

Package **substrate** (102)

First chip (106)

Ground bonding portion (112)

Tape (116)

Second chip (120)

Epoxy molding compound (126)

pp; 11 DwgNo 9/11

Technology Focus:

TECHNOLOGY FOCUS - POLYMERS - Preferred Component: The MCP comprises an epoxy molding compound (126) covering the first chip, tape and second chip.

ELECTRONICS - Preferred Component: The MCP comprises a ground bonding portion (112) on a second set of opposite sides of the **substrate** and coupled to the tape. A conductive wire electrically connects the bond pads of the first and second chips to the bond finger of the **substrate** . The package **substrate** is a **ball grid array substrate** . The tape is attached to the **surface** of the **first** chip excluding an area of the bond pads. It includes a first adhesive layer, conductive material layer and a second adhesive layer which are sequentially stacked. The first and second adhesive layers include conductive particles to improve **heat spread** . The tape includes a molding improving hole to alleviate thermal stress and to improve a molding property in a molding process. It extends from an edge of the **first** chip and attaches to the **surface** of the **substrate** including the ground bonding portion. The tape runs along a center axis of the first chip.

Preferred Dimension: The first and second adhesive layers each have a thickness of 5-50 microns. The conductive material layer has a thickness of 50-120 microns.

INORGANIC CHEMISTRY - Preferred Material: The particles are silver particles. The conductive material layer is an aluminum layer, a copper layer and/or a composite layer including the copper layer and a heat transfer improving layer formed on the copper layer.

ORGANIC CHEMISTRY - Preferred Material: The heat transfer improving

layer is a carbon layer or composite layer including carbon  
 Title Terms: PACKAGE; COMPRISE; TAPE; ATTACH; FIRST; CHIP; CONDUCTING;  
 MATERIAL; LAYER; ALUMINIUM; LAYER; COPPER; LAYER; COMPOSITE; LAYER;  
 COPPER; LAYER; HEAT; TRANSFER; IMPROVE; LAYER; FORMING; COPPER; LAYER  
 Derwent Class: A85; L03; U11  
 International Patent Class (Main): H01L-023/12; H01L-025/065; H05K-007/02  
 International Patent Class (Additional): H01L-023/34; H01L-025/07;  
 H01L-025/18; H05K-007/06; H05K-007/08; H05K-007/10  
 File Segment: CPI; EPI  
 Manual Codes (CPI/A-N): A12-E01; A12-E04; L04-C10; L04-C11D2; L04-C20A  
 Manual Codes (EPI/S-X): U11-D01A6; U11-E01B; U11-E02A2  
 Polymer Indexing (PS):  
 <01>  
 \*001\* 2004; P0464-R D01 D22 D42 F47  
 \*002\* 2004; ND01; Q9999 Q7330-R; Q9999 Q7523

22/9/4 (Item 4 from file: 350)  
 DIALOG(R) File 350:Derwent WPIX  
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015901654 \*\*Image available\*\*  
 WPI Acc No: 2004-059494/200406  
 XRAM Acc No: C04-024470  
 XRPX Acc No: N04-048121

**Thermally enhanced plastic ball grid array package for semiconductor industry, comprises heat sink having heat spreader stand-off sections with lower section the forms physical interface between heat spreader and substrate**

Patent Assignee: ST ASSEMBLY TEST SERVICES PTE LTD (STAS-N)  
 Inventor: APALE H T; BALANON G; SHIM I K  
 Number of Countries: 001 Number of Patents: 002  
 Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030197195	A1	20031023	US 2002119920	A	20020410	200406 B
US 6706563	B2	20040316	US 2002119920	A	20020410	200420

Priority Applications (No Type Date): US 2002119920 A 20020410

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030197195	A1		16	H01L-031/328	
US 6706563	B2			H01L-021/44	

Abstract (Basic): US 20030197195 A1

**NOVELTY** - A thermally enhanced plastic ball grid array package comprises heat sink for mounting over a surface of substrate of the package. The heat sink comprises horizontal section being parallel with substrate over which heat spreader is mounted; and heat spreader stand-off sections extending from perimeter of horizontal section. A lower section of heat spreader stand-off sections forms physical interface (42) between heat spreader and substrate.

**DETAILED DESCRIPTION** - A thermally enhanced plastic ball grid array (PBGA) package comprises a heat sink for mounting over a surface of a substrate of the PBGA package. The heat sink comprises a horizontal section being parallel with a substrate over which the heat spreader is mounted, the horizontal section having a perimeter; and heat spreader stand-off sections extending from the perimeter of the horizontal section. A lower section of the heat spreader stand-off sections forms a physical interface between the heat spreader and the substrate over which the heat spreader is

mounted. Each of the **heat spreader** standoff sections comprises an upper section connected with the horizontal section of the spreader under an angle; a center section connected with the upper section in a plane of the upper section; and a lower section connected with the center section of the **heat spreader** standoff section. Each lower section of each of the **heat spreader** standoff sections comprises a **first** horizontal section being parallel with the **surface** of the **substrate**. The **first** horizontal section is connected with the lower section of the **heat spreader** stand-off section. A U-shaped extension is connected with the first horizontal section, with a lower side of the U-shaped extrusion facing the **substrate**, with two retaining sides of the extrusion interfacing with the surface of the **substrate** under an angle, with at least one opening having been created through the lower side of the U-shaped extrusion. A second horizontal section is connected to the U-shaped extrusion.

An INDEPENDENT CLAIM is also included for packaging a **semiconductor** device, forming PBGA package, comprising providing a **semiconductor** device mounting support having a **first** and a **second surface**, the **semiconductor** device mounting support having been provided with interconnect traces and at least one metal pad; mounting at least one **semiconductor** device over the **second surface** of the **semiconductor** device mounting support; connecting the at least one **semiconductor** device in a face upward position by facing an active surface of the at least one **semiconductor** device away from the **semiconductor** device mounting support, using interconnect wires between the interconnect traces provided in the **semiconductor** device mounting support and contact points provided in an active surface of the **semiconductor** device; and positioning a **heat spreader** over the surface of the **substrate**.

USE - For **semiconductor** industry.

ADVANTAGE - The invention has low parasitic inductance, low cost, and does not require a redesign of the **substrate** over which the die is mounted while meeting conventional manufacturing standards.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of a PBGA package.

Physical interface (42)

pp; 16 DwgNo 2A/5

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The package additionally comprises a **substrate** having a **first** and a **second surface**, at least one metal pad having been provided over the **second surface** of the **substrate**, and at least one **semiconductor** device having been mounted and interconnected over the **second surface** of the **substrate**. The **heat spreader** has been positioned over the **second surface** of the **substrate**. The metal pad has been aligned with at least one opening created through the lower side of the U-shaped extrusion. It has been inserted into the opening created through the lower side of the U-shaped extrusion. At least one supply of thermally conductive epoxy is provided over the surface of the metal pad, thus at least overlying the lower side of the U-shaped extrusion with a layer of the thermally conductive epoxy. A stud bump is provided over the surface of the at least one metal pad having been aligned with the at least one opening created through the lower side of the U-shaped extrusion.

Preferred Method: The method additionally comprises curing the mold compound and the thermally conductive epoxy.

METALLURGY - Preferred Component: The metal pad comprises copper (Cu). The stud bump comprises gold or Cu. The metal pad serves as ground pad. The spreader comprises solder

Title Terms: THERMAL; ENHANCE; PLASTIC; BALL; GRID; ARRAY; PACKAGE;



**SEMICONDUCTOR ; INDUSTRIAL; COMPRISE; HEAT; SINK; HEAT; SPREAD; STAND;  
SECTION; LOWER; SECTION; FORM; PHYSICAL; INTERFACE; HEAT; SPREAD;  
SUBSTRATE**

Derwent Class: A32; A85; L03; U11  
International Patent Class (Main): H01L-021/44; H01L-031/328  
File Segment: CPI; EPI  
Manual Codes (CPI/A-N): A05-A01E2; A11-B01; A12-E07C; L04-C25  
Manual Codes (EPI/S-X): U11-D01A3; U11-D02B2  
Polymer Indexing (PS):

<01>

\*001\* 2004; P0464-R D01 D22 D42 F47; S9999 S1434

\*002\* 2004; ND01; ND07; Q9999 Q7476 Q7330; B9999 B5527 B5505; N9999  
N6440-R; K9416

22/9/5 (Item 5 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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015668523 \*\*Image available\*\*

WPI Acc No: 2003-730710/200369

XRAM Acc No: C03-200936

XRPX Acc No: N03-584074

**Anchoring heat spreader of plastic ball grid array package to  
underlying substrate surface involves aligning anchor posts over  
substrate surface with openings provided through contact surface of  
stand-off features of heat spreader**

Patent Assignee: ST ASSEMBLY TEST SERVICES PTE LTD (STAS-N); ST ASSEMBLY  
TEST SERVICES LTD (STAS-N)

Inventor: APALE H T; AQUIEN W; ARARAO V; FILOTEO D; MERILO L; SHIM I K

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030138994	A1	20030724	US 200255094	A	20020123	200369 B
US 6737298	B2	20040518	US 200255094	A	20020123	200433

Priority Applications (No Type Date): US 200255094 A 20020123

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

US 20030138994 A1 16 H01L-021/44

US 6737298 B2 H01L-021/44

Abstract (Basic): US 20030138994 A1

**NOVELTY - Heat spreader (14) of plastic ball grid array  
(PBGA) package (10) is anchored to an underlying substrate (12)  
surface by aligning anchor posts over the substrate surface with  
openings provided through a contact surface of stand-off features (38)  
of the heat spreader .**

**DETAILED DESCRIPTION - Anchoring heat spreader of plastic ball  
grid array package to un underlying substrate surface of the PBGA  
package involves providing a substrate for a PBGA package, where the  
substrate has been provided with heat spreader anchor posts over  
the substrate surface where the heat spreader anchor posts are  
separated by a first distance; providing a heat spreader for a  
PBGA package, where the heat spreader comprises a horizontal  
portion parallel with the substrate surface, heat spreader  
stand-off features having a contact surface that provide contact  
between the heat spreader and the substrate , and the contact  
surface of the heat spreader stand-off features have been provided  
with openings; aligning the anchor posts over the surface of the**

**substrate** with openings provided through the contact surface provided through the contact surface of stand-off features of the **heat spreader** ; and inserting the anchor post provided over the surface of the **substrate** into the openings provided through the contact surfaces of the stand-off features of the **heat - spreader** , creating anchor posts protruding through the opening provided through the contact surfaces.

An INDEPENDENT CLAIM is also included for a method for creating a PBGA package.

USE - For anchoring a **heat spreader** of a PBGA package to the underlying **substrate** surface of the PBGA package.

ADVANTAGE - The invented method allows for quick and reliable positioning and anchoring of the **heat spreader** over the **substrate** surface of the package.

DESCRIPTION OF DRAWING(S) - The figure shows a first flow of creating a PBGA package.

PBGA) package (10)

**Substrate** (12)

**Heat spreader** (14)

Addition layer (37)

Stand-off features (38)

pp; 16 DwgNo 7g/8

#### Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The anchor posts comprise deposits of thermally and electrically conductive material.

Preferred Method: A layer of electrically and thermally conductive material is deposited over the anchor posts protruding through the openings provided through the contact surfaces to include a surface area of the **heat spreader** surrounding the openings provided through the contact surfaces. The deposited layer of electrically and thermally conductive material is deposited.

POLYMERS - Preferred Material: The anchor posts are made of epoxy to which traces of silver have been added and solder paste and a solid metal. The electrically conductive material comprises epoxy to which traces of silver have been added

Title Terms: ANCHOR; HEAT; SPREAD; PLASTIC; BALL; GRID; ARRAY; PACKAGE; UNDERLYING; **SUBSTRATE** ; SURFACE; ALIGN; ANCHOR; POST; **SUBSTRATE** ; SURFACE; OPEN; THROUGH; CONTACT; SURFACE; STAND; FEATURE; HEAT; SPREAD  
Derwent Class: A85; L03; U11

International Patent Class (Main): H01L-021/44

International Patent Class (Additional): H01L-021/48; H01L-021/50

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A05-A01E2; A12-E07C; L04-C25

Manual Codes (EPI/S-X): U11-D01A3; U11-D01A5; U11-D02B; U11-E02A3

Polymer Indexing (PS):

<01>

\*001\* 018; P0464-R D01 D22 D42 F47

\*002\* 018; ND01; Q9999 Q7476 Q7330; B9999 B3269 B3190; B9999 B5527 B5505; B9999 B5414-R B5403 B5276

\*003\* 018; R05319 D00 D09 Ag; A999 A135

22/9/6 (Item 6 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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015491531 \*\*Image available\*\*

WPI Acc No: 2003-553678/200352

XRAM Acc No: C03-149583

XRPX Acc No: N03-439515

**Packaging of semiconductor device by forming internal mold cap over semiconductor device, forming external mold cap surrounding internal mold cap and placing a heat spreader**

Patent Assignee: ST ASSEMBLY TEST SERVICES LTD (STAS-N)

Inventor: BALANON G; CHOW S G; SHIM I K

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6534859	B1	20030318	US 2002116983	A	20020405	200352 B

Priority Applications (No Type Date): US 2002116983 A 20020405

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6534859	B1	14	H01L-023/495		

Abstract (Basic): US 6534859 B1

NOVELTY - Packaging of **semiconductor** device comprises mounting a **semiconductor** device over a mounting support, forming an internal mold cap over the device with an opening, forming an external mold cap surrounding the internal mold cap with a cavity separating the external cap from the internal cap, dispensing thermally conductive epoxy in the opening and the cavity and placing a **heat spreader**.

DETAILED DESCRIPTION - Packaging of **semiconductor** device comprises providing Front-Of-Line processing of **semiconductor** device(s) mounted on a mounting support. An external layer of mold compound with a **first** height is created over a **second surface** of the mounting support. It is created in a closed loop form at the periphery of the mounting support. The external layer of mold compound is kept out from the **semiconductor** device and interconnect wires (46, 48) to the **semiconductor** device. An internal layer of mold compound with a **second** height is created over the **second surface** of the support overlying and surrounding the **semiconductor** device. Opening(s) provided in the internal layer of mold compound further encases the **semiconductor** device and the interconnect wires to the **semiconductor** device in the internal layer of the mold compound. A cavity is provided between the internal and external layers of the mold compound. The **second** height is lower than the **first** height. External **surfaces** of the external layer of mold compound intersect the mounting support under an angle. Layers of thermally conductive epoxy (58) are dispensed in the opening and in the cavity. A **heat spreader** (60) is provided over the surface of the external layer of the mold compound for converting the internal layer into an internal mold cap (80) and the external layer into an external mold cap (56, 82). A **first surface** of the **heat spreader** faces the **semiconductor** device and has protrusion(s) aligned with the **semiconductor** device. The mold compound is cured concurrent with curing the thermally conductive epoxy.

An INDEPENDENT CLAIM is also included for a **semiconductor** device package comprising a **semiconductor** device mounting support, an external layer of mold compound, an internal layer of mold compound, layers of **thermally** conductive epoxy and a **heat spreader**. The mold compound is cured at the same time as the thermally conductive epoxy.

USE - The invention is used for packaging a **semiconductor** device (claimed), particularly a PGBA package.

ADVANTAGE - The invention has improved thermal performance and enhanced electrical performance.

DESCRIPTION OF DRAWING(S) - The figures show a cross section after positioning a **heat spreader** and a top view of the package during

formation of internal and external mold caps.

Interconnect wires (46, 48)

Contact balls (50)

External mold cap (56, 82)

Conductive epoxy (58)

**Heat spreader** (60)

Internal mold cap (80)

pp; 14 DwgNo 5, 10a/10

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: The external layer is used as dam during the dispensing of the thermally conductive epoxy layers.

Preferred Method: An end-of-line processing is provided by connecting contact balls (50) to the **first surface** of **semiconductor** device, and completing creation of the plastic **ball grid** array (PGBA) package. A ground plane surrounding the **semiconductor** device is formed by filling the cavity with an electrically conductive epoxy. An electromagnetic interference shield is formed by filling the cavity with an electrically conductive epoxy.

POLYMERS - Preferred Materials: The **heat spreader** comprises a **thermally** conductive epoxy.

Title Terms: PACKAGE; **SEMICONDUCTOR** ; DEVICE; FORMING; INTERNAL; MOULD; CAP; **SEMICONDUCTOR** ; DEVICE; FORMING; EXTERNAL; MOULD; CAP; SURROUND; INTERNAL; MOULD; CAP; PLACE; HEAT; SPREAD

Derwent Class: A32; A85; L03; T05; U11

International Patent Class (Main): H01L-023/495

International Patent Class (Additional): H01L-021/50; H01L-023/10;

H01L-023/28

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A05-A01E2; A09-A03; A11-B05; A11-C02C; A12-E04;

A12-E07C; L04-C21; L04-C25

Manual Codes (EPI/S-X): T05-H08A; U11-D01A3; U11-D01A5; U11-D01C6;

U11-D02B1; U11-E02A1

Polymer Indexing (PS):

<01>

\*001\* 018; P0464-R D01 D22 D42 F47; M9999 M2073; L9999 L2391; L9999 L2073

\*002\* 018; ND01; ND07; N9999 N6177-R; Q9999 Q9381 Q7330; B9999 B3281

B3190; B9999 B5527 B5505; B9999 B3269 B3190; N9999 N6440-R

22/9/7 (Item 7 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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014678379 \*\*Image available\*\*

WPI Acc No: 2002-499436/200253

XRPX Acc No: N02-395429

Heat spreader substrate **structure for semiconductor package, has** substrate **which is located on upper surface of first heat** spreader , **wherein opening of first heat spreader is exposed**

Patent Assignee: ADVANCED SEMICONDUCTOR ENG INC (ADSE-N); CHAO S (CHAO-I);

LIAO K (LIAO-I)

Inventor: JAU S; LIAU G; CHAO S; LIAO K

Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020053731	A1	20020509	US 2001882012	A	20010615	200253 B
TW 457663	A	20011001	TW 2000123557	A	20001108	200253
US 6624523	B2	20030923	US 2001882012	A	20010615	200364

Priority Applications (No Type Date): TW 2000123557 A 20001108

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020053731	A1		10	H01L-023/10	
TW 457663	A			H01L-023/28	
US 6624523	B2			H01L-023/48	

Abstract (Basic): US 20020053731 A1

NOVELTY - A second heat spreader (304) is fitted tightly into the opening (306) of a first heat spreader (302). The second heat spreader is thinner than the first heat spreader, and the lower surfaces of both heat spreaders are coplanar. A substrate (310) is located on the upper surface of the first heat spreader, wherein the opening of the first heat spreader is exposed.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a semiconductor package.

USE - For semiconductor packages, such as BGA package.

ADVANTAGE - Provides heat spreader substrate structure that reduces thickness of packaging.

DESCRIPTION OF DRAWING(S) - The figure is a schematic cross-sectional view of a semiconductor in a packaging process.

First heat spreader (302)

Second heat spreader (304)

Opening (306)

Substrate (310)

pp; 10 DwgNo 3/11

Title Terms: HEAT; SPREAD; SUBSTRATE; STRUCTURE; SEMICONDUCTOR; PACKAGE; SUBSTRATE; LOCATE; UPPER; SURFACE; FIRST; HEAT; SPREAD; OPEN; FIRST; HEAT; SPREAD; EXPOSE

Derwent Class: U11; V04

International Patent Class (Main): H01L-023/10; H01L-023/28; H01L-023/48

International Patent Class (Additional): H01L-023/36; H01L-029/40

File Segment: EPI

Manual Codes (EPI/S-X): U11-E02A3; V04-M05

22/9/8 (Item 8 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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014384307 \*\*Image available\*\*

WPI Acc No: 2002-205010/200226

XRAM Acc No: C02-062823

XRPX Acc No: N02-156005

Manufacture of substrate e.g. cavity-down plastic ball - grid -array substrate for packaging semiconductor involves forming cavity in substrate, surface pre-treatment, stencil-printing, curing and thermal lamination

Patent Assignee: VIA TECHNOLOGIES INC (VIAT-N); CHIEN R (CHIE-I)

Inventor: CHIEN C; CHIEN R

Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020009826	A1	20020124	US 2001828858	A	20010410	200226 B
TW 445558	A	20010711	TW 2000106982	A	20000414	200226
US 6566166	B2	20030520	US 2001828858	A	20010410	200336

Priority Applications (No Type Date): TW 2000106982 A 20000414

Patent Details:

Patent No	Kind	Lang	Pg	Main IPC	Filing Notes
US 20020009826	A1		17	H01L-051/40	
TW 445558	A			H01L-021/60	
US 6566166	B2			H01L-021/44	

Abstract (Basic): US 20020009826 A1

**NOVELTY** - A **substrate**, e.g. cavity-down plastic **ball - grid** -array (CD-PBGA) **substrate**, having organic **substrate** (62) and **heat spreader** (64) is manufactured by forming a cavity (66) in a middle region of an organic **substrate**, and sequentially performing **first surface** -pre-treatment, **second surface** -pre-treatment, **first** stencil-printing, curing and **first** thermal lamination.

**DETAILED DESCRIPTION** - Manufacture of a **substrate**, e.g. CD-PBGA **substrate**, having organic **substrate** and **heat spreader** includes forming a cavity in middle region of the organic **substrate**, and sequentially performing (i) a **first surface** pre-treating process to form a **first** oxide layer, (ii) a **second surface** pre-treating process to form a **second** oxide layer, (iii) a first stencil-printing process to form a liquid-type adhesive layer, (iv) a first curing process to reduce lamination fluidity of adhesive layer and (v) a first thermal-lamination process to bond the first oxide layer to the laminating side of **heat spreader**. The organic **substrate** comprises conductive pads, first copper layer and conductive vias. The first copper layer and the vias act to electrically connect the conductive pads. The **heat spreader** is made of copper alloys and comprises a laminating side and a **heat - spreading** side. The **first** oxide layer is formed on **surface** of the **first** copper layer and increases the adhesion of organic **substrate surface**. The **second** oxide layer is formed on the laminating side of **heat spreader** and increases the adhesion of **heat spreader**. The adhesive layer is formed outside of a predetermined area on the second layer. The size and the position of predetermined area correspond to organic **substrate** cavity that is arranged to receive an integrated circuit ( IC ) die.

**USE** - The method is used for manufacturing a **substrate** useful in packaging a **semiconductor** device, e.g. CD-PBGA **substrate** for **ball grid** array ( BGA ) packaging.

**ADVANTAGE** - The method is simple, and production costs are reduced. The efficiency and reliability of the product are improved.

**DESCRIPTION OF DRAWING(S)** - The figure shows the CD-PBGA **substrate**

Organic **substrate** (62)  
**Heat spreader** (64)  
 Cavity (66)  
 IC die (68)  
 Buffer layer (92)  
 Heat-dissipating pads (94)  
 pp; 17 DwgNo 5/15

Technology Focus:

**TECHNOLOGY FOCUS** - **ELECTRONICS** - Preferred Method: Nickel/gold plating is carried out after thermal lamination to form a nickel layer on conductive pads and a gold layer on nickel layer. A second stencil-printing is conducted form a buffer layer (92) in predetermined area of **heat spreader**, and a second curing process is performed to solidify the buffer layer. The buffer layer increases the adhesion of IC die to **heat spreader** at high temperature.

The **second** stencil-printing is conducted between **second surface** pre-treatment and **first** stencil-printing. Heat-dissipating pads (94) are positioned in the buffer layer to transmit heat generated by the IC die (68) to the **heat spreader**. The **heat** -dissipating

pads cover 0-90% of the surface of predetermined area. They are formed from nickel and gold layers deposited on the **heat spreader**. A third stencil-printing is performed to form a passivation layer on the **heat - spreading** side of the **heat spreader**, and a third curing process is performed to solidify the passivation layer.

The third stencil-printing is performed between **second surface** pre-treatment and **first** stencil-printing. A thermal treatment is performed between **first surface** pre-treatment and thermal lamination to remove moisture in the organic **substrate** and to shrink the organic **substrate** to control **substrate** warpage after thermal lamination. The thermal treatment may be performed after thermal lamination to cure the adhesive layer and to adjust warpage of **substrate**.

Preferred Components: The buffer layer comprises black ink layer, and the passivation layer comprises liquid ink layer. The organic **substrate** also includes second copper layer(s).

Title Terms: MANUFACTURE; **SUBSTRATE**; CAVITY; DOWN; PLASTIC; BALL; GRID; ARRAY; **SUBSTRATE**; PACKAGE; **SEMICONDUCTOR**; FORMING; CAVITY; **SUBSTRATE**; SURFACE; PRE; TREAT; STENCIL; PRINT; CURE; THERMAL; LAMINATE

Derwent Class: L03; U11

International Patent Class (Main): H01L-021/44; H01L-021/60; H01L-051/40

International Patent Class (Additional): H01L-021/48; H01L-021/50

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L04-C22

Manual Codes (EPI/S-X): U11-D01A3; U11-D01C6; U11-D02B1

22/9/9 (Item 9 from file: 350)

DIALOG(R) File 350:Derwent WPIX

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014342404 \*\*Image available\*\*

WPI Acc No: 2002-163107/200221

XRAM Acc No: C02-050281

XRPX Acc No: N02-124466

**Low-profile semiconductor device, e.g. ball grid array device, includes second encapsulant formed to encapsulate solder balls or lumps with bottom ends exposed to and flush with bottom surface of second encapsulant**

Patent Assignee: UNITED TEST CENT INC (UNTE-N)

Inventor: BAI J; TSAI C; TSAI T

Number of Countries: 029 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6326700	B1	20011204	US 2000639202	A	20000815	200221 B
EP 1205973	A1	20020515	EP 2000124579	A	20001110	200239 N
TW 452903	A	20010901	TW 2000116410	A	20000815	200244 N
KR 2002037454	A	20020522	KR 200067325	A	20001114	200277 N

Priority Applications (No Type Date): US 2000639202 A 20000815; EP

2000124579 A 20001110; TW 2000116410 A 20000815; KR 200067325 A 20001114

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

US 6326700 B1 11 H01L-023/29

EP 1205973 A1 E H01L-023/31

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT  
LI LT LU LV MC MK NL PT RO SE SI TR

TW 452903 A H01L-021/60

KR 2002037454 A H01L-023/12

Abstract (Basic): US 6326700 B1

NOVELTY - A low-profile **semiconductor** device has a **substrate**, a **semiconductor** die, gold wires and solder balls or lumps, and two encapsulants. The second encapsulant is formed over the conductive traces of the **substrate** to encapsulate the conductive traces, gold wires, a hole, and solder balls or lumps with bottom ends exposed to or flush with a bottom **surface** of the **second** encapsulant.

DETAILED DESCRIPTION - A low-profile **semiconductor** device comprises a **substrate** (41), a **semiconductor** die (40), gold wires and solder balls or lumps, and two encapsulants. The **substrate** has a base layer and conductive traces formed on the base layer. The base layer is formed with at least a hole. The **semiconductor** die has an active surface and an opposing inactive surface. It is mounted on the base layer of the **substrate** via the active surface. The gold wires pass through the hole in the **substrate** for electrically coupling the **semiconductor** die to the conductive traces on the **substrate**. The solder balls or lumps are arranged on terminals of the conductive traces for electrically connecting the **semiconductor** die to external devices. The first encapsulant is formed on the **substrate** to encapsulate the **semiconductor** die. The second encapsulant is formed over the conductive traces of the **substrate** to encapsulate the conductive traces, the gold wires, and the hole. It is also formed to encapsulate solder balls or lumps with bottom ends exposed to and flush with the bottom **surface** of the **second** encapsulant. An INDEPENDENT CLAIM is also included for a method of manufacturing a low-profile **semiconductor** device.

USE - As low-profile **semiconductor** device, e.g. ball grid array devices.

ADVANTAGE - The device has a reduced overall thickness. It eliminates warpage of the device such that the occurrence of delamination between the **semiconductor** die and the **substrate** can be effectively prevented. It can improve the accuracy of testing of electrical performance. It can be electrically connected to an external device in a quality-assured way than the prior art. The **substrate** of the device needs not to be coated with solder mask, thus reducing the cost for making the **substrate**.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of a **semiconductor** device.

**semiconductor** die (40)  
**substrate** (41)  
upper encapsulant (43)  
**heat spreader** (46)  
top surface (430)  
pp; 11 DwgNo 6/11

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The lumps formed by printing or plating methods. The inactive surface of the **semiconductor** die is exposed to top surface (430) of the upper encapsulant (43) or covered by the upper encapsulant. The **substrate** is formed with two holes parallelly arranged or with four holes in a rectangular arrangement. A **heat spreader** (46) is attached to the inactive surface of the **semiconductor** die or to the base layer of the **substrate** and formed with an opening for the **semiconductor** die to be received. The method also includes grinding the second encapsulant and solder balls or lumps to reduce the thickness of the second encapsulant and the heights of the solder balls or lumps, subsequent to the formation of the second encapsulant. The gold wires are pre-encapsulated with encapsulating resin to hermetically seal the gold wires, subsequent to the step of electrically coupling the



**semiconductor** die to the conductive traces of the **substrate** via the gold wires.

INORGANIC CHEMISTRY - Preferred Material: The lumps are made of copper, aluminum, copper alloy, aluminum alloy, or tin/lead alloy  
Title Terms: LOW; PROFILE; **SEMICONDUCTOR** ; DEVICE; BALL; GRID; ARRAY; DEVICE; SECOND; ENCAPSULATE; FORMING; ENCAPSULATE; SOLDER; BALL; LUMP; BOTTOM; END; EXPOSE; FLUSH; BOTTOM; SURFACE; SECOND; ENCAPSULATE  
Derwent Class: L03; U11  
International Patent Class (Main): H01L-021/60; H01L-023/12; H01L-023/29; H01L-023/31  
File Segment: CPI; EPI  
Manual Codes (CPI/A-N): L04-C17A; L04-C21  
Manual Codes (EPI/S-X): U11-D01A7; U11-E02A1

22/9/10 (Item 10 from file: 350)  
DIALOG(R) File 350:Derwent WPIX  
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013771770 \*\*Image available\*\*  
WPI Acc No: 2001-255981/200126  
XRPX Acc No: N01-182425

**BGA semiconductor package having exposed heat dissipation layer and its manufacturing method without the need of opening a hole on the substrate for heat sink insertion**

Patent Assignee: SILICONWARE PRECISION IND CO LTD (SILI-N)  
Inventor: HE T; KE J; LAI J; LUO S; HO T; KO E; LAI J Y; LO R H Y  
Number of Countries: 002 Number of Patents: 002  
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
TW 413874	A	20001201	TW 99105757	A	19990412	200126 B
US 6282094	B1	20010828	US 2000545996	A	20000410	200151

Priority Applications (No Type Date): TW 99105757 A 19990412

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 413874	A		21	H01L-021/60	
US 6282094	B1			H05K-007/20	

Abstract (Basic): TW 413874 A

NOVELTY - There is disclosed a **BGA semiconductor package** having exposed heat dissipation layer and its manufacturing method. A **substrate** having a **first surface** and a **second surface** is provided and at least one die is adhered to the **first surface**, so that the die is electrically connected to the conductive trace formed on the **first surface** of the **substrate** via solder wires or solder balls. Then, a packaging resin is used to encapsulate the die and the **first surface** of at least part of the **substrate**. Next, there are conductive solder balls and heat solder balls arranged in an array manner and formed on the **second surface** of the **substrate** by soldering, so that the conductive solder balls are electrically connected to the conductive trace of the **substrate** via passing through the conductive through holes of the **substrate**, and the heat solder balls are thermally connected to the die via passing through the heat through holes of the **substrate**. A **heat dissipation layer** is **spread** on the area of the **second surface** of the **substrate** disposed with the heat solder balls, so as to integrally connect the heat solder balls to form a heat dissipation structure. Accordingly, the heat dissipation area and the exposed surface area are greatly increased, thereby effectively increasing the heat dissipation

efficiency of **semiconductor** packages without changing the  
manufacturing process and apparatus. Thus, manufacturing cost is low.  
pp; 21 DwgNo 1/6

Title Terms: **SEMICONDUCTOR** ; **PACKAGE**; **EXPOSE**; **HEAT**; **DISSIPATE**; **LAYER**;  
**MANUFACTURE**; **METHOD**; **NEED**; **OPEN**; **HOLE**; **SUBSTRATE** ; **HEAT**; **SINK**; **INSERT**  
Derwent Class: U11  
International Patent Class (Main): H01L-021/60; H05K-007/20  
International Patent Class (Additional): H05K-007/20  
File Segment: EPI  
Manual Codes (EPI/S-X): U11-D01A3

22/9/11 (Item 11 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
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013652310 \*\*Image available\*\*  
WPI Acc No: 2001-136522/200114  
XRPX Acc No: N01-099297

Heat spreader for a ball and grid array package with a chip attached  
to a first surface of a substrate by adhesives uses a substrate  
with two surfaces with solder balls formed on it and soldered to another  
device

Patent Assignee: CAESAR TECHNOLOGY INC (CAES-N)  
Inventor: LI J  
Number of Countries: 001 Number of Patents: 001  
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6163458	A	20001219	US 99453439	A	19991203	200114 B

Priority Applications (No Type Date): US 99453439 A 19991203  
Patent Details:  
Patent No Kind Lan Pg Main IPC Filing Notes  
US 6163458 A 4 H05K-007/20

Abstract (Basic): US 6163458 A

NOVELTY - The **heat spreader** for a ball and grid array package  
with a chip attached to a **first surface** of a **substrate** by  
adhesives uses a **substrate** with two surfaces with solder balls formed  
on it and soldered to another device. A chip (30) is attached in the  
cavity (12) in the **first surface** by adhesive. A **heat spreader**  
covers the chip, with a protuberance formed on the **heat spreader**  
contacting the chip.

USE - As a **heat spreader** for a ball and grid array package with  
a chip attached to a 1st surface of a **substrate** by adhesives.

ADVANTAGE - Protuberances on the **heat spreader** contacts the  
chip to enhance the **heat** dissipation effect of the chip.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross sectional  
view of the **ball grid** array packaged device.

the chip (30)  
the cavity (12)  
pp; 4 DwgNo 2/2

Title Terms: **HEAT**; **SPREAD**; **BALL**; **GRID**; **ARRAY**; **PACKAGE**; **CHIP**; **ATTACH**; **FIRST**;  
**SURFACE**; **SUBSTRATE** ; **ADHESIVE**; **SUBSTRATE** ; **TWO**; **SURFACE**; **SOLDER**; **BALL**;  
**FORMING**; **SOLDER**; **DEVICE**  
Derwent Class: U11; V04  
International Patent Class (Main): H05K-007/20  
File Segment: EPI  
Manual Codes (EPI/S-X): U11-D01A3; U11-D01A5; U11-D02B1; V04-Q02A; V04-T03

22/9/12 (Item 12 from file: 350)  
DIALOG(R) File 350:Derwent WPIX  
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013083711 \*\*Image available\*\*  
WPI Acc No: 2000-255583/200022  
XRAM Acc No: C00-077909  
XRPX Acc No: N00-189954

**Forming thermal conductive structure on printed circuit board ( PCB ) includes forming a heat spreader on its surface, forming a glue layer over the heat spreader and attaching a surface metallic layer to the spreader and the glue layer**

Patent Assignee: WORLD WISER ELECTRONICS INC (WORLD-N)  
Inventor: JEN J; TZENG T; CHENG D C H; TSENG T  
Number of Countries: 002 Number of Patents: 002  
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6032355	A	20000307	US 98130360	A	19980806	200022 B
TW 388201	A	20000421	TW 98106140	A	19980422	200061

Priority Applications (No Type Date): TW 98106140 A 19980422

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 6032355	A	11	H05K-003/34	
TW 388201	A		H05K-007/20	

Abstract (Basic): US 6032355 A

**NOVELTY** - A thermal conductive structure is formed on a **PCB** comprises forming a **heat spreader** (402) having an embossed pattern formed on its surface, after which an adhesive glue layer (404) is attached to the **heat spreader**. A surface metallic layer (406) is attached to the **heat spreader** and the glue layer, in which a portion of its layer is in direct contact with the **heat spreader**.

**DETAILED DESCRIPTION** - A method of manufacturing a thermal conductive structure on a **PCB**, comprises (a) attaching a **heat spreader** formed on the **PCB**; (b) forming a **first** embossed pattern on a portion of the **surface** of the **heat spreader**; (c) forming a **second** embossed pattern on the edge portion of the **surface** of the **heat spreader**; (d) forming an adhesive glue layer to the **heat spreader**; (e) attaching a surface metallic layer to the **heat spreader** and the adhesive glue layer, where a portion of the surface metallic layer is in direct contact or almost direct contact with the first and the second embossed portions of the **heat spreader**; and (g) mounting an external **heat sink** (514) on top of the **surface** metallic layer where corresponding to the **second** embossed pattern of the edge of the **heat spreader**.

**USE** - The method is used for forming a thermal conductive structure on a **PCB**. The thermal conductive structure can also be applied to **ball grid** array packages, chip scale packages and multi-chip modules.

**ADVANTAGE** - The thermal conductive path dissipating heat is reduced considerably and the resulting heat dissipation is very much faster. Since no extra material is required for forming these structures and the method of fabrication is quite simple, the structure can be mass-produced at a very low cost.

**DESCRIPTION OF DRAWING(S)** - The figure shows a cross-sectional view showing a package structure having an additional external heat sink.

**Heat spreader** (402)  
**Adhesive glue layer** (404)

Surface metallic layer (406)  
Heat sink (514)  
pp; 11 DwgNo 5/8

Technology Focus:

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The method further includes attaching a silicon chip to a chip mount pad region on the top surface of the surface metallic layer, where corresponding to the embossed pattern of the **heat spreader**. Preferred Steps: The step of forming an embossed pattern on the metallic **heat spreader** further includes using photolithographic and etching methods to form a number of through holes before using the same method to form the embossed pattern on its surface. The step of attaching the surface metallic layer on the **heat spreader** includes using vacuum pressure and/or a hot adhesive glue.

METALLURGY - Preferred **Heat Spreader**: The **heat spreader** is formed from a material that includes a metallic layer.

CERAMICS AND GLASS - Preferred **Heat Spreader**: The **heat spreader** is also formed from a material that includes a ceramic layer.

POLYMERS - Preferred **Heat Spreader**: The **heat spreader** could also be formed from a material that includes a polymer layer.

Title Terms: FORMING; THERMAL; CONDUCTING; STRUCTURE; PRINT; CIRCUIT; BOARD  
; **PCB**; FORMING; HEAT; SPREAD; SURFACE; FORMING; GLUE; LAYER; HEAT;  
SPREAD; ATTACH; SURFACE; METALLIC; LAYER; SPREAD; GLUE; LAYER

Derwent Class: L03; V04

International Patent Class (Main): H05K-003/34; H05K-007/20

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L03-G; L03-H04E1

Manual Codes (EPI/S-X): V04-R14; V04-T03A

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